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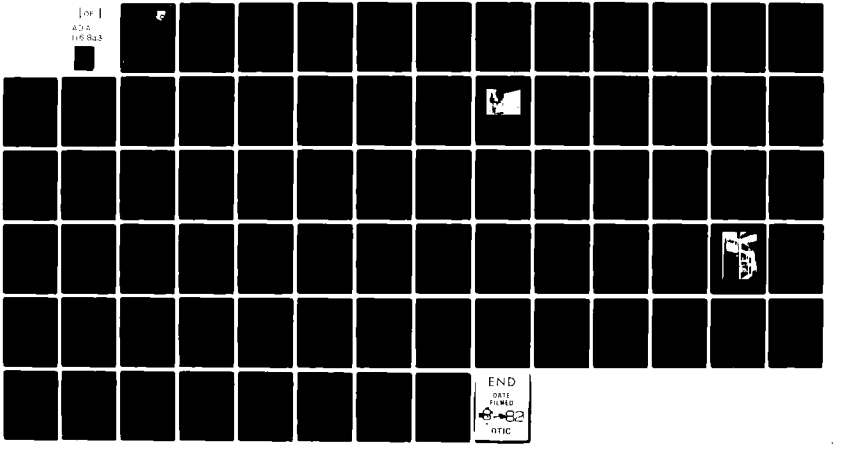

AFWAL-TR-82-1020

GaAs SURFACE PASSIVATION FOR DEVICE APPLICATIONS

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265

March 1982

Final Report for period 15 June 1978 through 15 June 1981

Approved for public release; distribution unlimited

AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
Wright-Patterson Air Force Base, OH 45433

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FOR THE COMMANDER

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This report describes the progress achieved during a three-year program to develop deposited dielectrics for GaAs device applications. Three applications of dielectrics have been investigated within this program: (1) isolation of control electrodes, (2) passivation of the GaAs surface, and (3) encapsulation of completed circuits. Deposition techniques employed were plasma-enhanced deposition (PED), pyrolytic chemical vapor deposition (CVD), and photo-chemical deposition (PCD). Plasma-enhanced

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dielectrics suitable for applications (1) and (3) were developed under Hughes internal funding early in the course of the program. Accordingly, the program was streamlined to concentrate on application (2).

The major thrust of this program was to evaluate the application of silicon nitride, germanium nitride, and silicon germanium nitride dielectrics prepared by PED and CVD to passivation of GaAs for insulated gate device applications. An extensive parametric study of the PED silicon nitride process was the largest single task of the program. Sixty-five deposition runs were performed using a high-vacuum compatible PED system developed under Hughes internal funding.

The overall process involves cleaning the sample, anodic oxidation of the GaAs surface, stripping the anodic oxide, an optional final wet-chamical surface preparation step, pre-deposition plasma-enhanced treatment of the walls of the deposition system or "preburn" (which may involve a concurrent sample surface treatment), optional plasma etching of the sample surface, and deposition of the dielectric. We have analyzed the effects of variations in (i) oxide stripping and final wet-chemical preparation procedures, (ii) preburn, (iii) plasma etches, (iv) deposition procedures, and (v) post-deposition thermal annealing on the electrical properties of the GaAs/silicon nitride interface.

Performing the preburn with the sample surface exposed to a plasma containing hydrogenerated species was found to be beneficial to the interface electrical properties as deduced by analysis of the capacitance-voltage and conductance-voltage behavior of GaAs metal-insulator-semiconductor capacitors.

Dramatic improvements in interface electrical properties were obtained by annealing GaAs/silicon nitride structures in nitrogen at temperatures up to 600°C for periods up to one hour.

Preliminary studies of pyrolytic silicon nitride/GaAs structures yielded electrical results consistent with the conclusion that inversion of the n-type GaAs surface can be achieved in this system.

Preliminary investigations of PED germanium nitride/GaAs and silicon germanium nitride/GaAs structures were performed. The best results, achieved with germanium nitride films deposited by reaction of germane with nitrogen, were inferior to our best PED silicon nitride results.

Attempts to prepare germanium nitride by CVD from germane and ammonia were unsuccessful.

PREFACE

The work reported here was supported by the Avionics Laboratory, Wright-Patterson Air Force Base, Ohio, under contract F33615-78-C-1444, Project Number 2305, Task 2305R1. The monitoring engineer was Capt. R.L. Johnson (AFWAL/AADR). The program objective was to investigate the passivation of gallium arsenide and the application of dielectric thin-film overlayers in metal-insulator-semiconductor field-effect transistors.

This work was performed jointly by Hughes Research Laboratories, Malibu, CA 90265 and the Technology Support Division of the Hughes Aircraft Company, Culver City, CA 90230. Contributions to this work were made by C.L. Anderson, M.D. Clark, R.A. Jullens, A.J. Mohr, J.W. Peters, and F.L. Gebhart.

This is the final report. The first, second, and third reports were published as AFAL-TR-79-1057, AFAL-TR-79-1234, and AFWAL-TR-80-1149, respectively, with the same title. This report covers the period from 15 June 1978 through 15 June 1981. The submittal date of this report was December 1981.

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SECTION 1

INTRODUCTION AND SUMMARY

The goal of this program was to develop dielectrics that will serve the following three purposes in gallium arsenide device technology:

- Passivation – reduction of the number of electrically active centers ("surface states") at the semiconductor surface so that the surface potential can be modulated by control electrodes ("gates") overlaying the dielectric.
- Isolation – insulation of control electrodes from each other and from the substrate.
- Encapsulation – overcoating of operational circuits to reduce their sensitivity to environmental influences.

To serve these three purposes, Hughes Aircraft Company is developing a variety of deposited dielectrics. Techniques for depositing these dielectric materials are being developed under Hughes internal funding. Evaluation and optimization of these materials for GaAs device applications was performed under the subject contract.

The following materials were originally proposed for development under this program:

- $Ga_xAl_yO_z$ (gallium-aluminum oxide), referred to as (Ga, Al)O
- $Ga_xSi_yO_z$ (gallium-silicon oxide), or (Ga, Si)O
- $Al_xSi_yO_z$ (aluminum-silicon oxide), or (Al, Si)O
- SiO_xN_y (silicon oxynitride)
- (Si,Ge)N (silicon-germanium nitride).

Three basic techniques for depositing these materials were originally proposed:

- Pyrolytic chemical vapor deposition (CVD)
- Plasma-enhanced deposition (PED)
- Photochemical deposition (PCD).

We reported (in AFAL-TR-79-1057) the successful use of a proprietary plasma-deposited glass as an isolation dielectric in GaAs MESFET ICs. This dielectric has been successfully used in all GaAs ICs prepared by the Hughes Aircraft Company for over three years. In AFAL-TR-79-1234, we reported the application of this dielectric as an encapsulant for discrete GaAs MESFETs. Four microwave GaAs FETs with 1 x 600 μm gates and mounted in NEC carriers were evaluated for microwave gain at 9.70 GHz before and after deposition of the dielectric glass. The results are presented in Table 1. On the basis of the four measurements on each device, the average gain degradation resulting from encapsulation was 0.45 dB. In view of the increased parasitic capacitance resulting from the presence of the glass, we feel this reduction in gain is very reasonable. Because of the demonstrated utility of this dielectric for isolation and encapsulation applications, this program was redirected to investigate the application of deposited dielectrics solely for passivation applications.

During the course of this program, a considerable body of experimental evidence was accumulated by ourselves and others indicating that oxidation of the GaAs surface leads to the development of high interface state densities near the middle of the GaAs bandgap and hence to interfacial electrical properties which are undesirable for insulated gate devices. Accordingly, all work on oxides as passivating layers for GaAs under this program was terminated during the fourth semester of this program.

During the final year of the program, the major emphasis was placed on a parametric study of procedures for preparing GaAs/silicon nitride structures by plasma-enhanced deposition.

This effort was by far the largest single endeavor during the course of the program and resulted in substantial improvement in the electrical quality of the GaAs/PED silicon nitride interface compared to that attainable at the outset. A description of this parametric study occupies a substantial portion of this report.

The overall process involves a significant number of steps including (a) cleaning of the water, (b) anodic oxidation of the wafer, (c) stripping of the oxide, (d) a final wet-chemical surface treatment (optional), (e) pre-deposition plasma treatment of the walls of the deposition system or "preburn" (which may include exposure of the wafer surface to the plasma), (f) plasma etching of the

TABLE 1. Response of GaAs FETs to Encapsulation

Device No.	Gate Bias, V	Drain Bias, V	Drain Current, mA	Input Power, dBm	Unencapsulated Gain at 9.70 GHz, dBm	Encapsulated Gain, dB	Gain Change, dB
1	-3.05	5.0	50	0	8.25	7.1	-1.15
	-1,62	5.0	90	+10	7.6	6.9	-0.7
2	-2.91	5.0	50	0	9.05	7.75	-1.3
	-1.56	5.0	90	+10	7.3	7.6	+0.3
3	-3.42	5.0	50	0	7.95	7.4	-0.55
	-2.02	5.0	90	+10	7.55	7.3	-0.25
4	-3.5	5.0	50	0	7.55	7.4	-0.15
	-1.96	5.0	90	+10	7.35	7.3	-0.05

wafer surface (optional), and (g) the actual dielectric deposition. A standard procedure for steps (a) through (c) leading to reproducible surface properties of the wafer as determined by ellipsometry was developed during the third semester of this program and was reported in the third interim report (AFWAL-TR-80-1149). A large-scale high-vacuum-compatible plasma-enhanced deposition system developed under Hughes internal funding was completed during the same period and applied to this program. A baseline process for steps (e) and (g) was developed under this program and was reported in the third interim report. A description of the baseline process is presented as Section 2 of the present report.

During the last year of this contract sixty-five PED silicon nitride deposition runs were performed to assess the effects of variations in steps (c), (d), (e), (f), and (g) on the electrical properties of the GaAs/PED silicon nitride interface. The results of this study, discussed in detail in Section 3 of this report, indicated that the electrical properties of this interface could be improved by optimization of the process. The most significant improvements were achieved by exposing the sample surface to hydrogenated species during the preburn stage.

Near the end of the present program we extended our study of the GaAs/PED silicon nitride interface by exploring thermal annealing of the samples prior to metal deposition for metal-insulator-semiconductor (MIS) capacitor formation. Dramatic improvements of interface electrical properties were achieved by subjecting the samples to relatively severe anneals – up to one hour at 600°C in flowing dry nitrogen. These preliminary studies, discussed in Section 4, were highly encouraging and provide a strong impetus for further exploration in this area.

During the course of this program we achieved some encouraging early results in our studies of the use of pyrolytically deposited silicon nitride for passivation of GaAs surfaces. MIS capacitors incorporating films prepared using our baseline CVD process exhibited electrical characteristics under illumination consistent with the interpretation that inversion of the n-type GaAs surface was being achieved. Later attempts to improve the quality of the interface between these films and n-type GaAs by post-deposition plasma annealing in hydrogen and by pre-deposition pyrochemical treatment were unsuccessful. The results of our investigations involving CVD silicon nitride are presented in Section 5.

A relatively limited number of experiments were performed to assess the utility of PED germanium nitride and silicon germanium nitride films for surface passivation of GaAs. Four deposition runs were performed to evaluate deposition of germanium nitride from germane and nitrogen; eight germanium nitride runs were performed using germane and ammonia. Four runs were performed to evaluate the deposition of silicon germanium nitride from silane, germane, and nitrogen. The best electrical results were obtained from germanium nitride films grown from germane and nitrogen. These results were comparable to some of the promising early PED silicon nitride results. Our experiences in this area are discussed in Section 6.

During the last six months of the program we also attempted to prepare germanium nitride films by pyrolysis of germane and ammonia. Seventeen deposition runs were performed. Although we explored extreme variations in process parameters such as the germane to ammonia ratio we were unable to prepare films with sufficient nitrogen content to be acceptable insulators. The details of these experiments are summarized in Section 7.

In the final section of this report, Section 8, we provide a brief assessment of the knowledge gained from this program and suggest directions for further study.

SECTION 2

BASELINE PLASMA-ENHANCED DEPOSITION PROCESS FOR SILICON NITRIDE

Much of the effort expended during the first two years of this program was directed towards development of a reliable process for preparing high-quality oxygen-free silicon nitride films by plasma-enhanced deposition (PED) and towards identification of wet-chemical surface preparation procedures which result in consistent surface properties of the GaAs wafers introduced into the PED system. Since most of the remainder of this report deals with the effect of variations of the sample preparation and deposition process on the electrical quality of the GaAs/Si_3N_4 interface, this section is provided to fully document the baseline process for reference purposes and to explain the rationale for this process. For those who wish to omit the discussion of the rationale for selection of the particular baseline process, a concise description of the process is provided in Section 2.C.

A. CLEANING AND ETCHING PROCEDURES

The application of deposited dielectric films to the passivation of GaAs for device applications relies on the premise that the surface "oxide" film of unknown composition that exists on the sample surface immediately prior to the deposition of the dielectric is sufficiently thin and tenuous that the surface properties can be controlled by the deposited dielectric. Accordingly, the development of surface cleaning and etching procedures which result in a thin "oxide" layer of reproducible properties was addressed during the third semester of this program and reported in AFWAL-TR-80-1149.

Prior to the final surface etching step, all samples were cleaned by a standard cleaning procedure designed to remove organic contaminants and any excess Ga on the wafer surface resulting from epitaxial growth. This cleaning procedure, which has been found to be successful for a wide variety of applications is described in Table 2.

To investigate the effectiveness of etching for minimizing residual oxide, we employed our Gaertner L116 ellipsometer to measure the apparent complex index of refraction, $N_s^* = N_s + iK_s$, of the substrate immediately after etching.

Neither the thickness nor the index, N_f, of a very thin-film can be precisely determined unless a true N_s^* is accurately known. Unfortunately, N_s^* is not known with sufficient accuracy to permit such a detailed analysis. However, the effect of a thin, transparent film on the measured N_s^* is to decrease N_s and increase $|K_s|$ over that of an ideal substrate ($K_s < 0$ for an absorbing substrate). This will be the case for $1 < N_f < N_s$, assuming $|K_s| \ll N_s$. From our measurements, together with published absorption data, our best estimate of the ideal N_s^* of GaAs at a 632.8 nm wavelength is 3.89 - 0.19i. For an oxide film, we expect $N_f < 3.89$ so that the effectiveness of an etch can be judged by the degree to which it minimizes $|K_s|$ and maximizes N_s. The value of K_s is the most sensitive indicator of a surface film.

The initial etches evaluated were NH_4OH:30% H_2O_2:H_2O (5:2:240 by volume) and 1 M NaOH:0.76M H_2O_2 (1:1 by volume). Ellipsometric analysis indicated that the NH_4OH:H_2O_2 etch leaves the least oxide, while the NaOH:H_2O_2 etch is slightly more uniform.

During our cleaning studies, we encountered several wafers of GaAs that were heavily contaminated with particulate matter and "scum" that had apparently resulted from the use of improper packing material by the suppliers. The solvent/HCl cleaning procedure of Table 2 was not completely effective for removing these heavy deposits since such deposits are not normally encountered on polished GaAs wafers. We found that most of the remaining contamination could be effectively removed by growing about 100 nm of native anodic oxide and then etching away the oxide with 1M NH_4OH. The oxide is grown at room temperature in an electrolyte of composition 17 g ammonium pentaborate per 100 ml of ethylene glycol. A proprietary method is used to electrically contact the backside of the wafer so that the entire front side can be anodized. To ensure uniformity, the wafer is illuminated during anodization. The cathode of the anodization cell is Pt foil.

Several etchants were evaluated on wafers that had received this additional anodization/stripping step after the Table 2 cleaning procedure. Effectiveness

TABLE 2. Cleaning Procedure for GaAs Wafers

Distinguish four categories and modify general cleaning procedure per instructions below.

A. New polished wafers

B. Epitaxial wafers

C. Ion implanted wafer not yet annealed

D. Photoresist processed wafers

General Procedure:

1. Trichloroethylene (TCE) to boiling (boil 3 min)

2. TCE to boiling (boil 3 min)

3. Cold methanol/acetone dip (80% acetone/20% methanol)

4. DI H_2O rinse (1 min)

5. 50% HCl/DI H_2O rinse (3 min)

6. DI H_2O rinse (2 min)

7. Isopropyl to boiling (boil 2 min)

8. Blow or spin dry

9. Inspect

Category A: Complete procedure

Category B: Change step 5 only if excess Ga is present. Use hot 50% HCl/DI H_2O, but do not boil.

Category C: Eliminate steps 4 and 5.

Category D: Change step 3 to boiling acetone (3 min).

Note: Use only the following solvents and chemicals: Allied Chemical, Semiconductor Low Mobile Ion Grade Mallinckrodt, Transistor Grade

DI H_2O — 18 MΩ

Or as approved by supervisor.

of cleaning was judged by ellipsometry as described above. The following were etches evaluated:

(1)	NH_4OH:30% H_2O_2:H_2O	(5:2:240)
(2)	1 M NaOH:0.76 M H_2O_2	(1:1)
(3)	HCl:H_2O:30% H_2O_2	(1:1:"a few drops")
(4)	Br_2:CH_3OH	(1% Br_2 by volume)
(5)	HF:H_2O	(10% HF by volume)
(6)	HCl:H_2O	(50% HCl by volume)

Etches (5) and (6) attack native oxide but do not etch GaAs at room temperature. These etches generally give comparable results, although Br_2:CH_3OH is somewhat less effective than the others. However, when applied either to samples that have or have not been cleaned by anodic oxide growth and stripping, none of the etches give a surface significantly superior to that obtained by anodic cleaning only. Furthermore, etches (1) through (4), which attack GaAs, cause some degradation of surface morphology because of non-uniform etching, whereas anodic cleaning essentially replicates the original polished surface. Consequently, wet chemical cleaning by the procedures of Table 2 followed by anodic oxide growth and stripping without subsequent GaAs etching was selected as the baseline wafer preparation process.

B. DESCRIPTION OF THE HUGHES RESEARCH LABORATORIES PLASMA REACTOR

The quality of the PED films prepared for this contract improved significantly when construction of the new PED system shown in Figure 1 was completed. This system was built using Hughes internal funding. A photograph of the actual system, without the screen enclosure used to prevent interference of the rf with the control electronics, is provided in Figure 2. In this system, the reducing gases (silane, germane, etc.) are introduced through a side port, rather than through a tube passing down the axis on the rf coil. This arrangement reduces that amount of surface area in the most intensely excited region of the plasma and precludes the possibility of a plasma being generated within the delivery tube for the reducing gases.

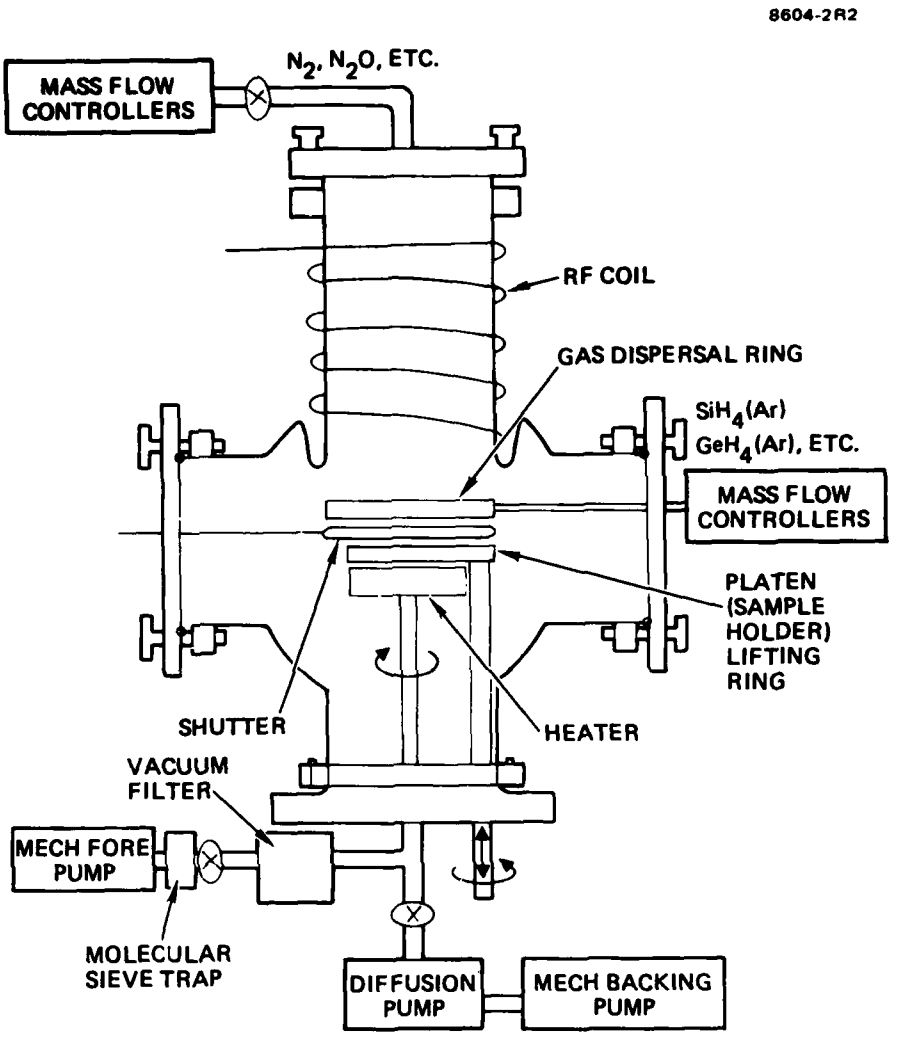

Figure 1. Schematic of the Hughes Research Laboratories deposition (PED) system.

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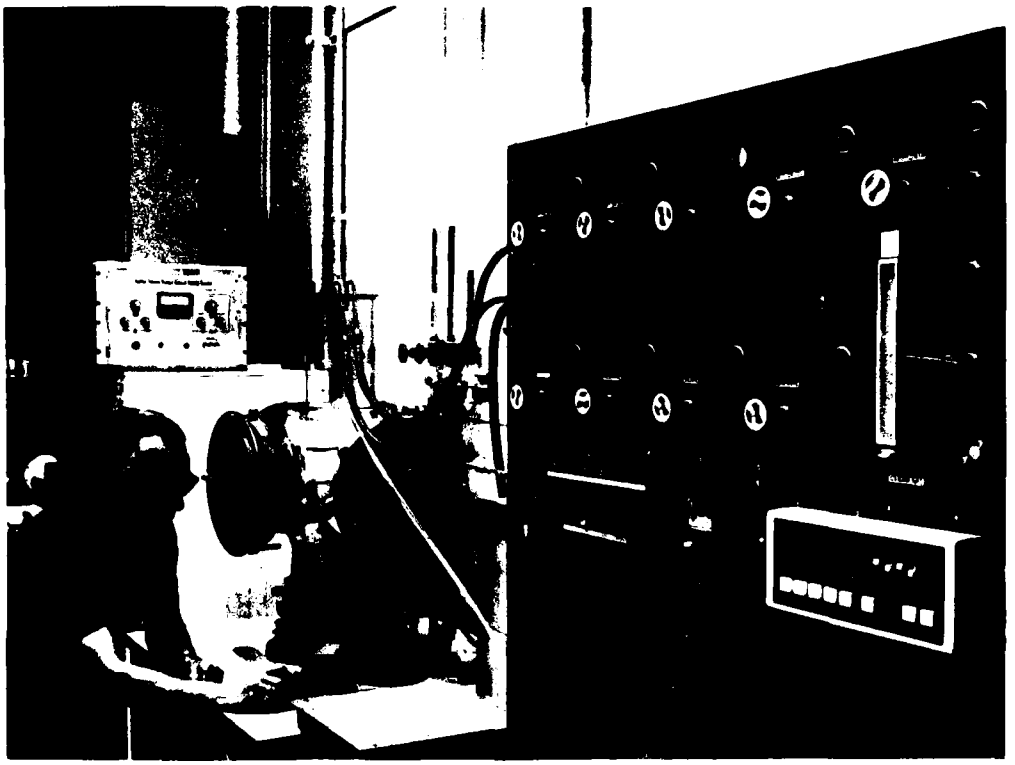

Figure 2. Large-scale high-vacuum-compatible plasma-enhanced-deposition system.

The dispersal ring for the reducing gases is attached to a bellows assembly and is capable of oscillating in both horizontal axes over the heater assembly. The heater itself is capable of rotation. The use of these mechanical motions results in very uniform deposition over large areas (typically ±2.5% over a 2-in. diameter wafer). Samples introduced into the system are placed on a 16-cm-diameter "platen" or sample holder which is capable of accepting four 5-cm-diameter circular wafers. The platen itself consists of a heavy Al annular ring over which a sheet of heavy Al foil is stretched and to which the Al foil is

clamped. During those stages of the deposition process which involve exciting the plasma, the platen rests on an Al sample heater. Because the sample heater tends to deform slightly at elevated temperatures, the use of a stretched Al foil membrane in the platen allows the platen to conform to the heater surface and results in superior thermal contact compared to that which would be achieved using a rigid platen.

The platen (sample holder) can be lifted off the heater using a lifting ring controlled by a push-pull/rotary feedthrough and removed from the system through the access door in the front of the chamber. During pumpdown, the platen can be positioned away from the heater to maintain a low sample temperature. Once high-vacuum conditions are achieved, the samples can be rapidly heated to deposition temperature by placing the sample holder plate onto the heater assembly. This provision reduces the possibility of baking contaminants onto the sample surface prior to deposition.

A mechanical shutter is provided to permit covering the sample during a "preburn" procedure used to outgas the chamber before deposition. The central chamber itself is a large sphere to reduce outgassing of the walls resulting from the proximity to the heater assembly.

During a typical deposition cycle, the system is evacuated to high vacuum conditions ($<5 \times 10^{-5}$ mm Hg, or 7×10^{-3}/Pa) before reactive gases are introduced. The diffusion pump is then valved off and the actual deposition is performed under evacuation by a large-capacity rotary pump protected by a vacuum particle filter. All gas flow rates are controlled by mass flow controllers. Deposition pressure is monitored by two capacitance manometer absolute pressure gauges. Because the accuracy of these gauges degrades after numerous depositions, a reference gauge, which is valved off during deposition cycles has been provided. It is used to calibrate the "working" gauge at periodic intervals.

C. DESCRIPTION OF BASELINE PROCESS

1. Stage 1: Anodic Cleaning

The GaAs wafer is wet-chemically cleaned using the procedure of Table 2.

2. Stage 2: Anodic Oxidation

The wafer is oxidized at room temperature in an electrolyte consisting of 17 g ammonium pentaborate dissolved in 100 ml of ethylene glycol. A proprietary method is used to contact the back side of the wafer electrically over a large area so that the entire front side can be anodized. To ensure uniformity the wafer is illuminated during anodization. The cathode of the anodization cell is Pt foil. Approximately 100 nm of native anodic oxide is grown using a current density of roughly 1 mA cm^{-2} and a final voltage of 50 V. Following anodization, the wafer surface is rinsed with 18 MΩ-cm deionized water and blown dry in filtered dry nitrogen. The oxidized surface of the wafer is then coated with a thick layer of photoresist which is allowed to air dry at room temperature. Typically, the wafer is then diced by scribing the back side and cleaving.

3. Stage 3: Oxide Stripping

Prior to deposition, the photoresist is stripped from the oxidized surface of the wafer with acetone. The anodic oxide is removed by a 2 min etch in 1 M NH_4OH. The sample is then rinsed in 18 MΩ-cm deionized water and blown dry in filtered dry nitrogen.

4. Stage 4: Final Wet-Chemical Treatment of Water Surface (optional)

This step is not performed in the baseline process.

5. Stage 5: Sample Loading

The sample is immediately loaded into the deposition system by placing it on the platen (sample holder) which has been pre-heated to 200°C. One variation from the baseline process which has been explored is loading the sample onto the platen while the platen is detached from the sample heater and is at room temperature. This condition is described in the tables in Section 3 as "cold platen".

Following sample loading, the system is roughed down using the large mechanical forepump; then the system is pumped down to high vacuum ($<5 \times 10^{-5}$ mm Hg or 7×10^{-3} Pa) using the diffusion pump and backing pump. In the "cold platen" cases the platen is placed on the sample heater after high vacuum conditions have been achieved. The high vacuum valve is then closed.

6. Stage 6: Nitrogen Plasma Preburn

The system is outgassed by performing a nitrogen plasma preburn. Nitrogen is admitted into the system through the mass flow control system. Simultaneously, the valve on the large forepump is opened. The nitrogen flow rate is allowed to stabilize, then the chamber pressure is regulated using the forepump valve as a throttle valve. The mechanical shutter over the sample is closed. The rf supply is then turned on, exciting the plasma.

Baseline preburn conditions are as follows:

N_2 flow rate	16 sccm
Chamber pressure	100 mTorr (13 Pa)
RF power	100 W
Hot plate temperature	200°C
Shutter position	Closed
Duration	10 min

Following the preburn the plasma is extinguished by turning off the rf supply. The nitrogen flow is then discontinued.

7. Stage 7: Plasma Etch (Optional)

This step is not performed in the baseline process. If employed, a plasma etch is performed in the same manner as the preburn except that an etching gas is admitted and the shutter is normally open to expose the sample to the etching plasma.

8. Stage 8: Deposition

Following the preburn (and plasma etch process if employed) the system is again pumped down to high vacuum by shutting the forepump valve and opening the high vacuum valve. When a pressure below 5×10^{-5} mm Hg (7×10^{-3} Pa) has been achieved, the high vacuum valve is closed again. Nitrogen and a gas mixture of 1.5% SiH_4 in Ar are admitted into the chamber through the mass flow control system. Simultaneously, the forepump valve is opened. Once the nigrogen and dilute silane flows have stabilized, the pressure is regulated using the forepump valve. The rf power supply is then turned on to ignite the plasma.

Baseline deposition conditions are as follows:

N_2 flow rate	16 sccm
Flow rate of 1.5% SiH_4 in Ar	90 sccm
Chamber pressure	250 mTorr (33 Pa)
RF power	30 W
Hot plate temperature	200°C
Hot plate rotation	on, 6 rpm
Shutter position	open
Duration	10 min

Following the deposition, the rf power supply is turned off. The nitrogen and dilute silane flows are then terminated and the system is allowed to pump down to forepump vacuum (a few micrometers of Hg). This step allows the dilute silane remaining in the system to be removed. The system is then vented to permit sample removal. These parameters result in a deposition rate of about 7.5 nm/min and consistently give films with refractive indices between 1.90 and 2.05 at a wavelength of 632.8 nm.

Using the above parameters, films were deposited on pyrolytic carbon and examined by Rutherford backscattering (RBS). The RBS data indicated a Si/N ratio appropriate for Si_3N_4 and an upper limit on the O/N ratio of about 0.08.

Capacitance-voltage (C-V) and conductance voltage (G-V) data for a typical n-GaAs/baseline PED silicon nitride/Al capacitor are shown in Figures 3(a) and 3(b), respectively. The vertical axis of the G-V figure is the capacitance equivalent of the conductance (i.e., G/ω, where ω is the angular frequency, and $\omega = 2\pi f$, where f is the conventional frequency). These data exhibit the typical problems associated with GaAs/dielectric interfaces. In particular, the C-V data exhibit strong frequency dependence of the accumulation capacitance.

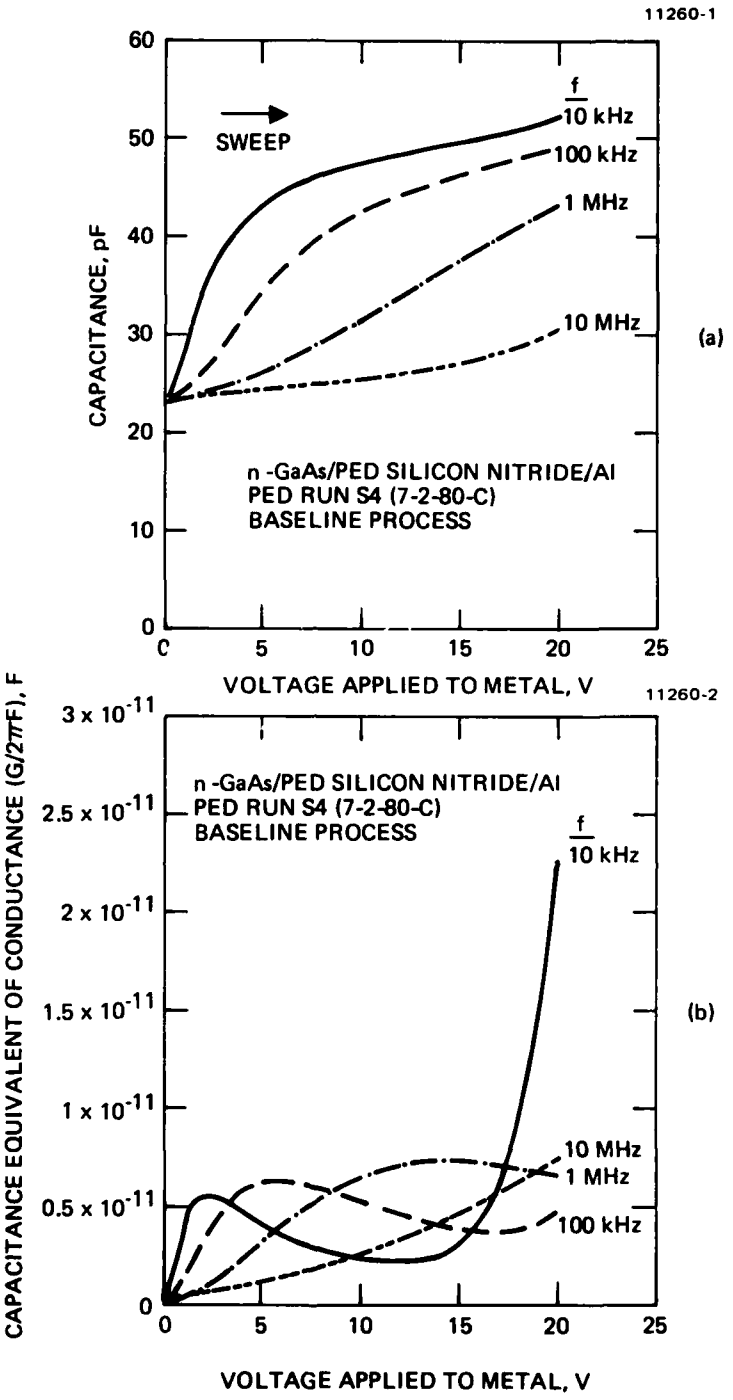

Figure 3. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric layer prepared by the baseline process.
(a) Capacitance voltage characteristics.
(b) Conductance voltage characteristics.

SECTION 3

PARAMETRIC STUDY OF THE EFFECTS OF PED PROCESS VARIATIONS ON THE ELECTRICAL PROPERTIES OF THE GaAs/PED SILICON NITRIDE INTERFACE

Sixty-five PED silicon nitride deposition runs were performed in an effort to identify process parameters which exhibit a significant influence on the electrical properties of the GaAs/PED silicon nitride interface. These runs can be conveniently grouped into four categories, based on the type of variation in the process involved in the respective runs. The process variations employed in each group are summarized as follows: (a) small variations in the standard procedure (loading procedure, temperature, silane flow rate); (b) preburn procedure; (c) final wet chemical treatment of the sample surface; and (d) plasma etching of the sample after preburn. The four groups are discussed individually in the following four subsections. In addition, samples from four runs were subjected to thermal annealing at temperatures up to 600°C. Samples from one of these runs exhibited the best interface electrical properties we have observed. Results of these annealing studies are presented in subsection 4.

A. RUNS INVOLVING SMALL VARIATIONS FROM STANDARD PROCEDURE

Ten runs were performed in this group. The variations from the baseline procedure employed in the individual runs are summarized in Table 3. Standard runs S4 and S8 yielded films with refractive indices of 2.12 and 2.06, respectively, with associated film thicknesses of 74 and 83 nm. The runs performed with 100 SCCM of the SiH_4/Ar mixture exhibited films with refractive indices of 2.17 and 2.02, with associated thicknesses of 85 and 95 nm. Run S7, performed with 80 SCCM SiH_4/Ar, produced a film with refractive index of 1.983 and thickness of 91 nm. Thus the optical properties and thickness of the deposited films are not strongly sensitive to the silane content of the plasma. None of the remaining runs of this group yielded films with refractive index or thickness outside the range encompassed by the six runs just described. Thus, the film properties are (fortunately) relatively insensitive to small variations in the baseline process.

TABLE 3. Deposition Conditions for Silicon Nitride Runs Exploring Small Variations from Standard Procedure

Run	Deviation from Standard Procedure
S1	cold platen
S2	100°C
S3	80 sccm SiH_4/Ar
S4	(standard run)
S5	100 sccm SiH_4/Ar
S6	300°C
S7	80 sccm SiH_4/Ar
S8	(standard run)
S9	100 sccm SiH_4/Ar
S10	300°C

Of the nonstandard runs in this group, the most promising from the point of view of interfacial properties were those performed at 300°C. The C-V and G-V characteristics from an n-GaAs/300°C PED Si_3N_4/Al capacitor from run S10 are shown in Figures 4(a) and 4(b), respectively. These data are qualitatively very similar to those of Figures 3(a) and 3(b) in that both samples exhibit substantial frequency dispersion of the accumulation capacitance and comparable conductance behavior (both in magnitude and variation with frequency). Thus, performing the preburn and deposition at 300°C yields comparable results to the standard 200°C process.

B. RUNS INVOLVING VARIATIONS IN PREBURN PROCEDURE

Thirty-two runs were performed to determine the effect of variations in the preburn procedure on interfacial electrical properties. Prior to initiating the first runs in this series, a revision was made in the baseline process: the second pumpdown of the system to high-vacuum conditions following the preburn was

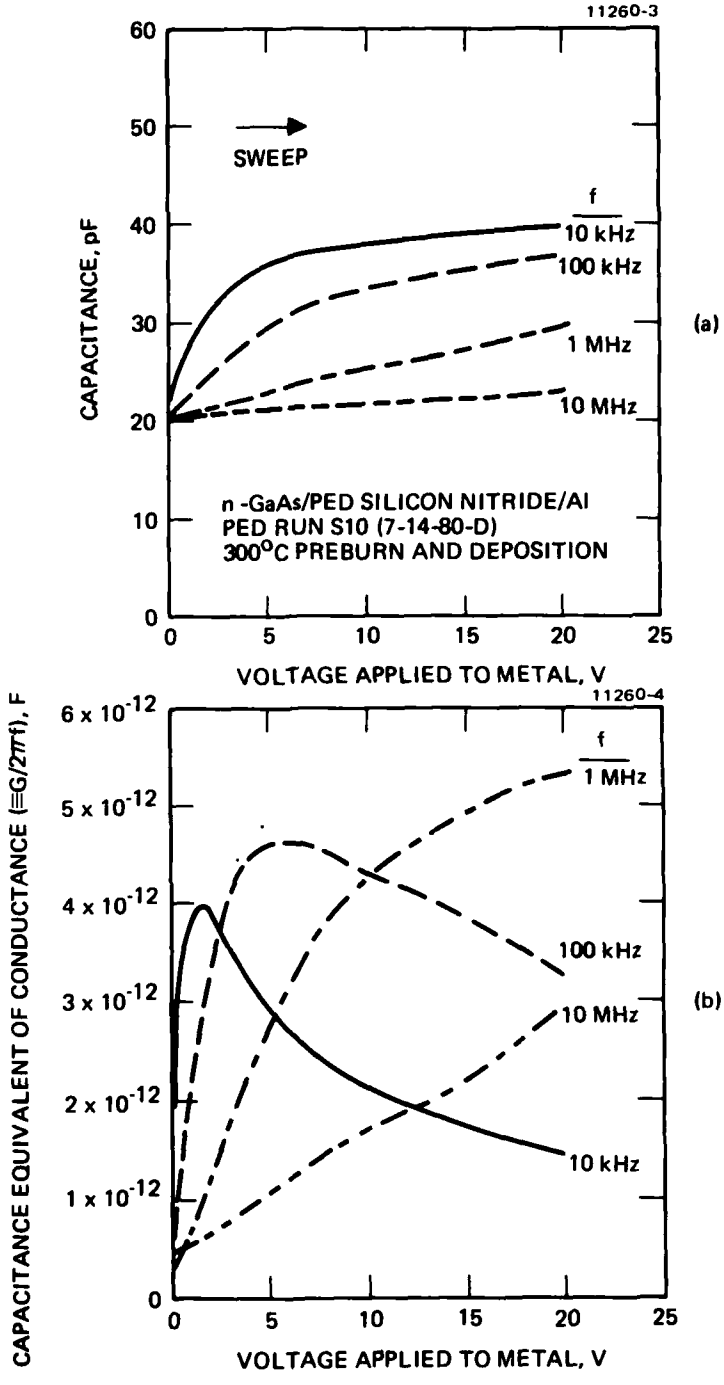

Figure 4. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric deposited at 300°C.
(a) Capacitance voltage characteristics.
(b) Conductance voltage characteristics.

eliminated. The motivation for this revision was that it reduced the total exposure time of the system to the ambient following the preburn, thereby reducing the extent of uncontrolled oxidation of the sample surface. There have been no observations that this revision of the standard procedure is either deleterious or beneficial; it does, however, simplify the deposition sequence, which is clearly desirable in its own right.

The deviations of each run in this group from the revised standard procedure are listed in Table 4. Most of the runs employed N_2 preburns. This group, however, also included preburns involving NH_3, H_2, and CF_4 gases. None of these gases is believed to etch GaAs in a plasma. Therefore, these runs are treated as involving preburn variations rather than plasma etch stages.

The primary observation to be made concerning runs for this group is that exposure of the sample surface to the preburn can be beneficial to the final electrical properties of the interface.

Figures 5(a) and 5(b) illustrate the electrical characteristics of an MIS capacitor incorporating a film grown on a sample which had been loaded cold, heated to 300°C after pumpdown to high vacuum, and exposed to a 2-min N_2 preburn (run S19). Compared to the data for a 300°C film deposited on a sample which had been covered during the preburn (Figures 4(a) and 4(b)), the data from run S19 exhibits reduced frequency dispersion between 10 kHz and 1 MHz, greater voltage dependence of the 10 MHz capacitance, narrower conductance peaks, and a peak in the 1 MHz conductance curve (not seen in Figure 4(b)). All of these features are indicative of a reduction in interface state density.

The effect of the duration of the exposure to the N_2 preburn is small, as can be seen from comparison of Figures 5(a) and 5(b) with Figures 6(a) and 6(b). In the latter case, the sample was exposed to a 10-min N_2 preburn. There is little qualitative difference between these data.

The second observation to be drawn from this group of runs is that preburns in hydrogenated gases can be beneficial. Of the runs involving preburns in gases other than N_2, the most promising was S50, in which the sample was exposed to a 5 min preburn in $N_2 + NH_3$ after a 5 min N_2 preburn with the shutter closed. Electrical data of MIS capacitors employing films from S50 (Figures 7(a) and 7(b)) are similar to those of Figures 5(a), 5(b), 6(a), and 6(b) except that the peak conductance values are substantially lower, and the conductance peaks occur at

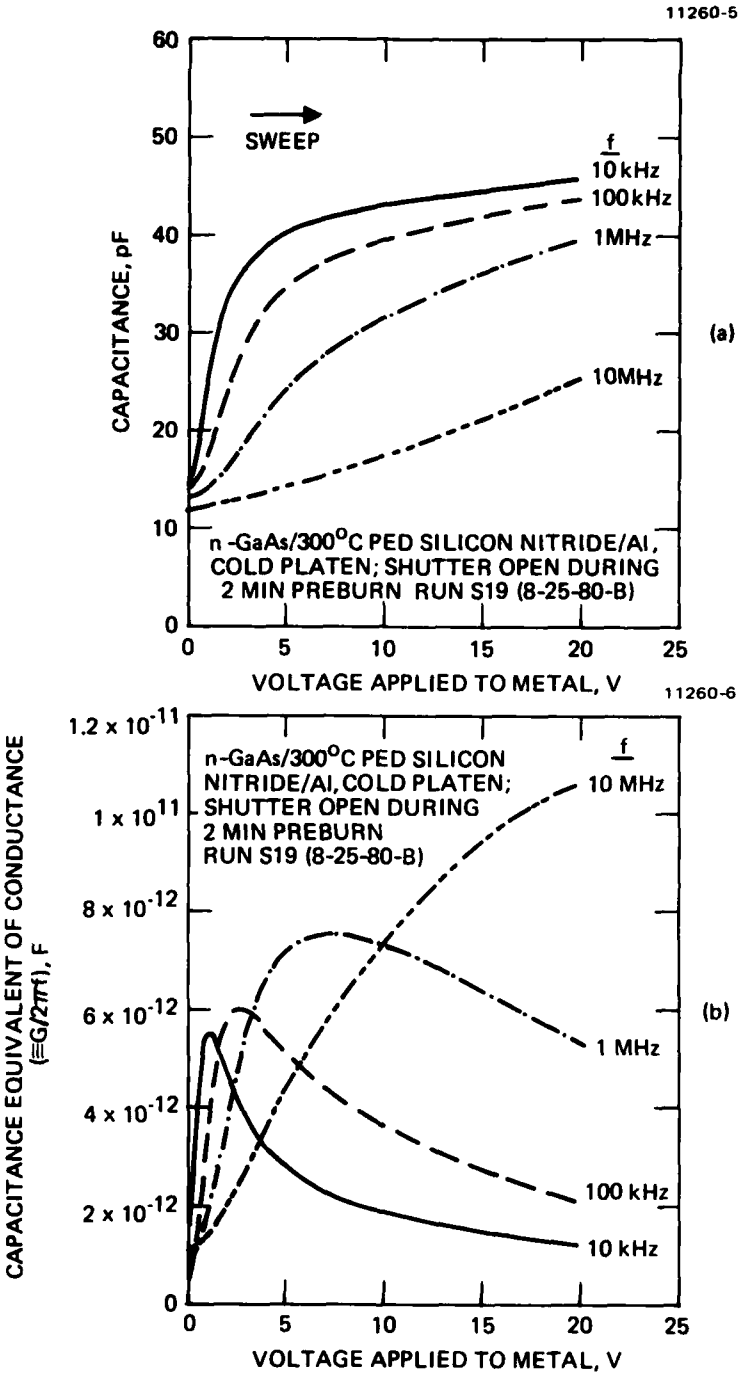

Figure 5. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited at 300°C after the sample had been loaded onto a cold sample holder heated to 300°C after pumpdown and exposed to a 2 min N_2 preburn.
(a) Capacitance voltage characteristics
(b) Conductance voltage characteristics

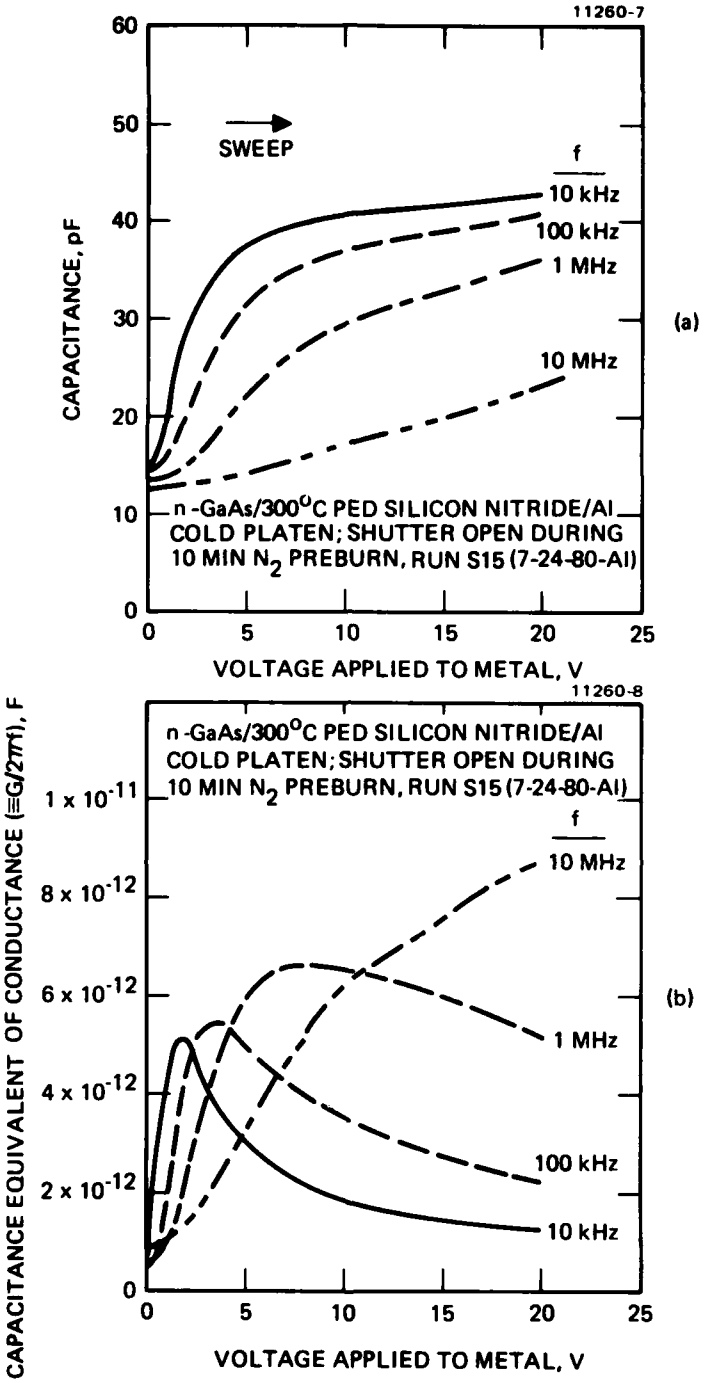

Figure 6. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor employing a dielectric deposited at 300°C after the sample had been loaded onto a cold sample holder, heated to 300°C after pumpdown and exposed to a 10 min N_2 preburn.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

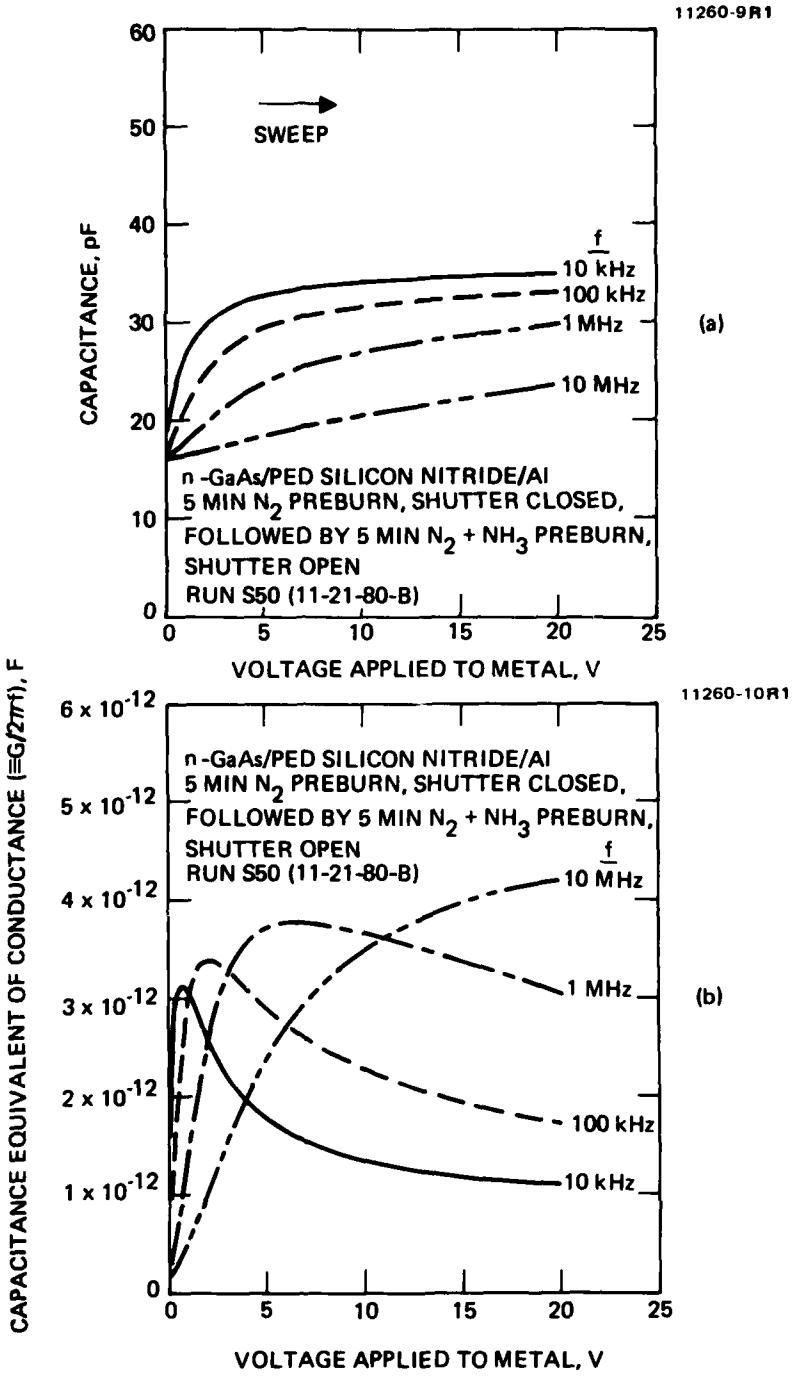

Figure 7. Characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited after a 5 min N_2 preburn with the shutter closed followed by a 5 min N_2 + NH_3 preburn with the shutter open.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

slightly lower voltages. (The capacitance values in Figure 7 are slightly lower than in Figures 5 and 6, but the ratio of conductance to capacitance in Figure 7 is definitely superior to those in the former two figures.) Thus the exposure to the mixed N_2 + NH_3 preburn appears to have resulted in improved interfacial properties.

C. RUNS INVOLVING VARIATIONS IN FINAL WET-CHEMICAL TREATMENT OF THE SAMPLE SURFACE

Eleven runs were performed involving variations in the final wet-chemical treatment of the GaAs surface prior to insertion into the vacuum chamber. The deviations of the deposition parameters for these runs from the revised standard procedure (baseline process without second pumpdown of system to high vacuum following preburn) are summarized in Table 5. For runs S24, S26, S28, S30, S31, and S32, the sample was dipped in methanol plus "a few drops" of HCl after the baseline oxide strip and placed in the deposition system wet. For run S36, the sample was dipped in methanol plus "a few drops" of HF after the baseline oxide strip and placed in the deposition system wet. For run S37, the anodic oxide was removed in HF:H_2O (1:9 by volume); the sample was then rinsed in 18 MΩ-cm deionized water and blown dry with filtered dry nitrogen gas before insertion into the deposition chamber.

Multifrequency C-V and G-V measurements were performed on MIS capacitors prepared from films deposited on n-GaAs samples in each run. None of these process variations resulted in any significant improvement in interface properties over those achieved by the baseline process (Figure 3).

D. RUNS INVOLVING PLASMA ETCHING OF THE SAMPLE AFTER PREBURN

Eight deposition runs plus two control runs (in which no deposition was performed) were carried out to analyze the effects of plasma etching of the sample surface with chlorinated species prior to deposition. The deviations of these eight runs from the revised standard procedure (baseline process without pumpdown to high vacuum following preburn) are summarized in Table 6.

TABLE 4. Deposition Conditions for Silicon Nitride Runs Exploring Variations in Preburn Procedure

Run	Deviations From Revised Standard Procedure (no second pumpdown)
S11	Shutter open during preburn
S12	Shutter closed during first minute of "deposition", then opened
S13	Room temperature; shutter open during preburn
S14	Room temperature; shutter closed during first minute of "deposition", then opened
S15	300°C; cold platen, shutter open during preburn
S16	300°C; cold platen, shutter open during 20 min preburn
S17	300°C; cold platen, no preburn
S18	300°C; cold platen, shutter open during 30 sec preburn
S19	300°C cold platen, shutter open during 2 min preburn
S20	300°C; cold platen, shutter open during NH_3 preburn
S21	300°C; cold platen, shutter open during 2 min NH_3 preburn
S22	300°C; cold platen, shutter open during 30 sec NH_3 preburn
S23	300°C; cold platen, 10 min NH_3 preburn
S29	Cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S33	300°C; cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S34	300°C; no preburn
S35	300°C; cold platen, no preburn
S38	CF_4 preburn (CF_4 fed through etching gas line)
S39	Cold platen, shutter open during 30 sec CF_4 preburn
S40	Cold platen, shutter open during CF_4 preburn
S43	Cold platen, shutter open during 20 W preburn
S44	Cold platen, no preburn, 500 mTorr deposition pressure

TABLE 4. Continued

Run	Deviations from Revised Standard Procedure (no second pumpdown)
S49	Mixed preburn — N_2 5 min then NH_3/N_2 5 min — run interrupted by mass flow-control failure
S50	5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 200 mTorr, followed by 5 min preburn, shutter open, in 16 sccm N_2 + 16 sccm NH_3, 200 W, 100 mTorr
S51	5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 16 sccm N_2 + 16 sccm NH_3, 300 W, 500 mTorr (uninterrupted repeat of S49)
S57	5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 18 sccm NH_3 + 18 sccm H_2, 200 W, 100 mTorr
S58	5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr followed by 5 min preburn, shutter open, in 18 sccm H_2, 200 W, 100 mTorr
S59	5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr followed by 10 min preburn, shutter closed, in 18 sccm H_2, 200 W, 100 mTorr
S60	30 sec 0.5% Br_2 in methanol oxide strip followed by methanol soak until loaded, 5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 16 sccm N_2 + 18 sccm NH_3, 200 W, 100 mTorr
S61	300°C; 5 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr, followed by 5 min preburn, shutter open, in 18 sccm H_2, 200 W, 100 mTorr
S63	300°C; 2 min NH_4OH:30% H_2O_2:H_2O (5:2:240) etch of non-anodized sample followed by deionized water rinse, cold platen, 10 min preburn, shutter closed, in 16 sccm N_2, 100 W, 100 mTorr, followed by 20 min preburn, shutter open, in 18 sccm H_2, 200 W, 180 mTorr
S65	Repeat of run S63

The initial experiments were done with pure CCl_4. Rapid etching was observed, along with visual evidence of a surface residue. The presence of a dielectric residue was verified by observation of MIS structure capacitances much lower than would be expected for the SiN_x dielectric alone. The MIS capacitors also exhibited high leakage and high ac loss. The etching residue was thought to be polymerized decomposition products of the etch gas. Nitrogen was added to etch gas in an unsuccessful attempt to eliminate the residue.

Results obtained in other Hughes projects indicated that CCl_2F_2 was superior to CCl_4 for GaAs plasma etching. Furthermore, less residue was expected with CCl_2F_2 since the fluoride compounds of carbon are generally more volatile than the chloride compounds. A mixture of 1.6 sccm CCl_2F_2 + 16 sccm N_2 was used at 100 mTorr pressure and 30 W rf power for etch times of 15 sec and 2 min. Capacitance data showed little evidence of a dielectric residue, but, as with CCl_4 etching, leakage and ac loss were so high that measurements for accumulation bias greater than ~3 V could not be made.

During the last six months of this program two runs were performed to explore the effects of HCl plasma treatments. Run S62 employed a 15 sec plasma etch of the sample surface. In run S64 an "HCl doped" film was prepared by starting the deposition with a gas mixture of 16 sccm N_2 + 90 sccm of 1.5% SiH_4 in Ar + HCl (controlled by an uncalibrated micrometer needle valve). The HCl flow was terminated immediately after turning on the rf power to start the deposition.

In contrast to the negative results obtained with CCl_4 and CCl_2F_2, neither of the runs employing HCl plasma treatments yielded pathological results. Electrical characteristics of a GaAs/PED silicon nitride/Al capacitor incorporating dielectrics from runs S62 and S64 are presented in Figures 8(a), 8(b), and 9(a) and 9(b), respectively. Comparison of Figures 8(a) and 8(b) with Figures 3(a) and 3(b) clearly indicates that the film deposited after HCl plasma etching exhibits inferior interfacial properties compared to the film prepared by the baseline process. The frequency dispersion of the accumulation capacitance of the HCl-etched sample is much more severe than the baseline sample. In addition, the conductance of the HCl etched sample exhibits a peak only at 10 kHz.

The sample incorporating an HCl "doped" dielectric (Figures 9(a) and 9(b)), however, exhibits interfacial properties which are somewhat superior to the baseline sample. The frequency dispersion of the accumulation capacitance of the

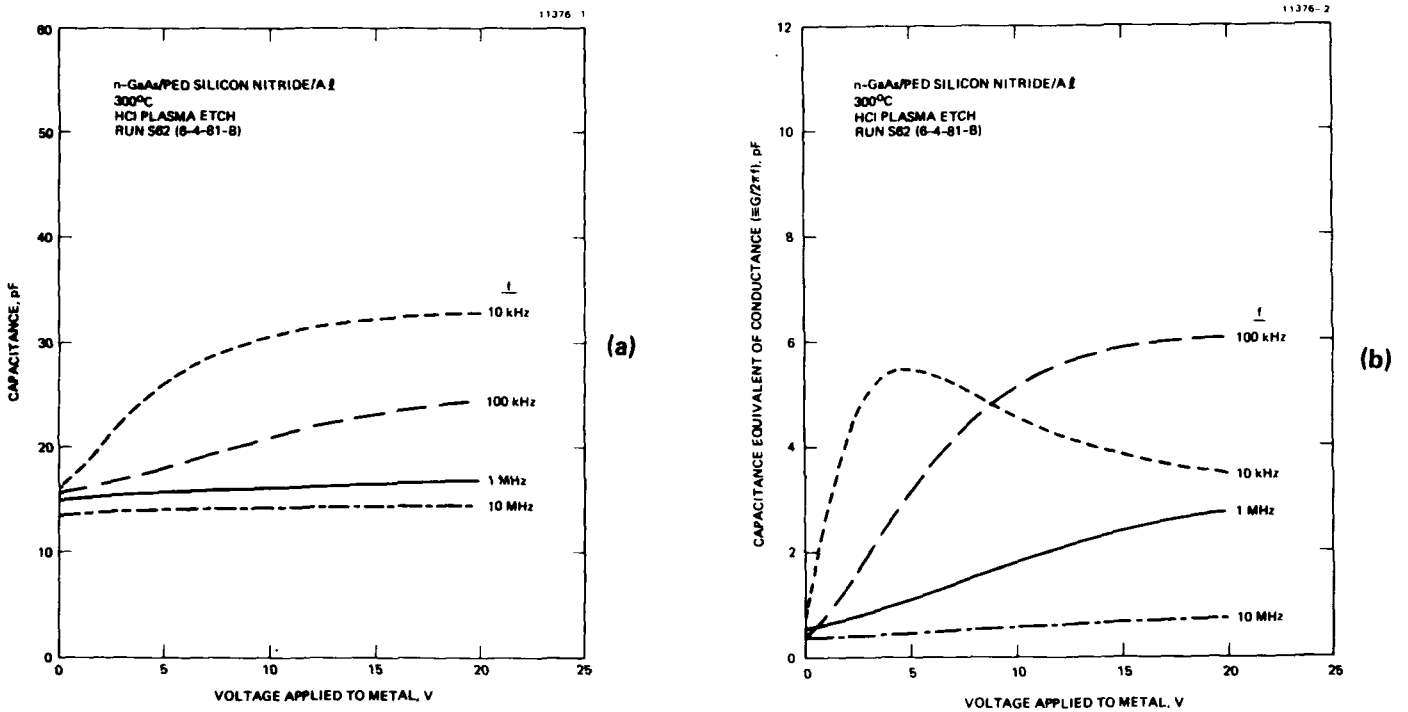

Figure 8. Electrical characteristics of an n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric grown at 300°C on a GaAs sample plasma etched with HCl.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

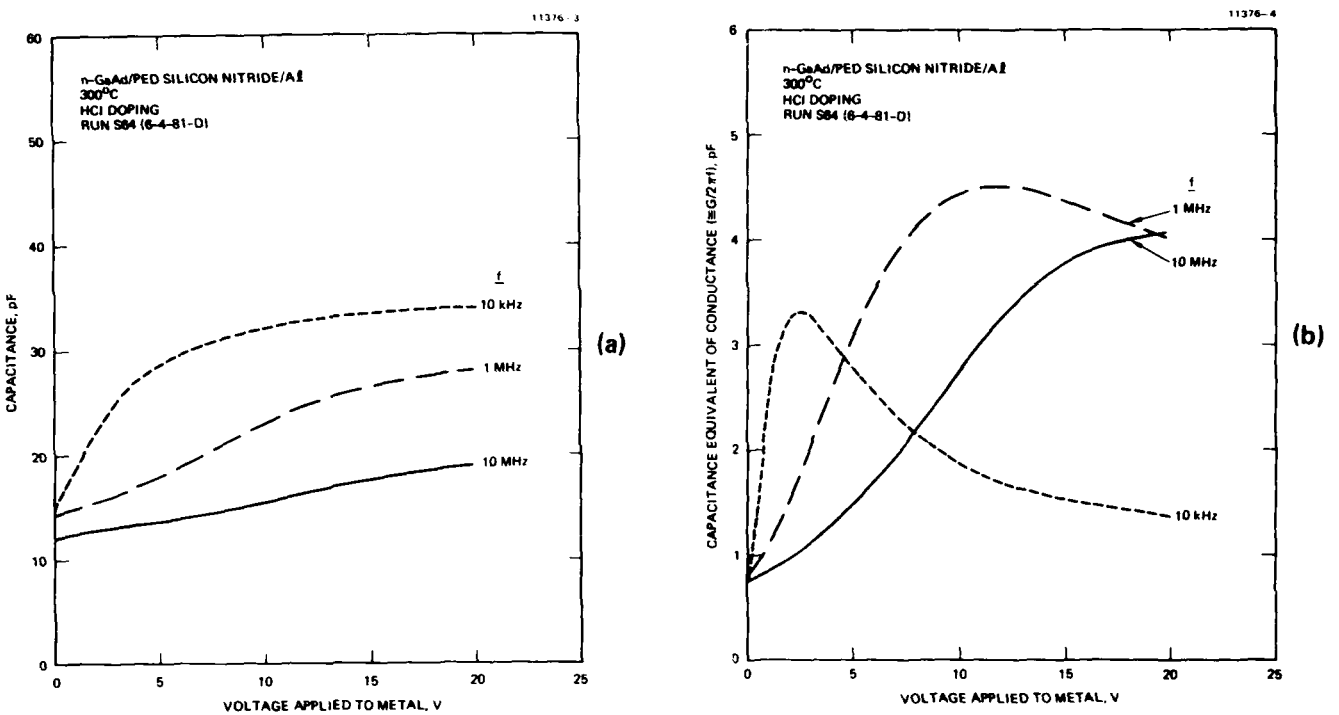

Figure 9. Electrical characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric grown at 300°C with HCl "doping" (see text for details).
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

HCl doped sample is smaller than that of the baseline sample. In addition, the capacitance of the HCl doped sample saturates somewhat more strongly in the accumulation regime than does that of the baseline sample. The conductance peaks of the HCl doped sample are slightly narrower than those of the baseline sample.

TABLE 5. Deposition Conditions for Silicon Nitride Runs Exploring Variations in Final Wet Chemical Treatment of Sample Surface

Run	Deviation From Revised Standard Procedure (no second pumpdown)
S24	300°C; dip in methanol + HCl after oxide strip, cold platen, no preburn
S251	300°C; 1 M HCl oxide strip, cold platen, no preburn
S26	Dip in methanol + HCl after oxide strip, cold platen, no preburn
S27	1 M HCl oxide strip, cold platen, no preburn
S28	Dip in methanol + HCl after oxide strip, cold platen, no preburn, Shutter closed during first minute of "deposition", then opened
S30	300°C; dip in methanol + HCl after oxide strip, cold platen, no preburn, shutter closed during first minute of "deposition", then opened
S31	300°C; dip in methanol + HCl after oxide strip, cold platen, NH_3 preburn
S32	300°C; dip in methanol + HCl after oxide strip, cold platen
S36	300°C; dip in methanol + HF after oxide strip, cold platen, no preburn
S37	300°C; HF oxide strip, cold platen, no preburn
S41	5 min NH_4OH: 30% H_2O_2:H_2O (5:2:240) oxide strip, cold platen, no preburn
S42	5 min NH_4OH: 30% H_2O_2:H_2O (5:2:240) oxide strip followed by methanol dip, cold platen, no preburn

TABLE 6. Deposition Conditions for Silicon Nitride Runs Exploring Plasma Etching of Wafer Surface After Preburn

Run	Deviations From Revised Standard Procedure (no second pumpdown)
S45	CCl_4 plasma etch, shutter open, 30 W, 50 mTorr, 1 min
S46	CCl_4 plasma etch, shutter open, 100 W, 100 mTorr, 1 min
S47	CCl_4 plasma etch, shutter closed, 30 W, 50 mTorr, 30 sec
S48	CCl_4 + N_2 plasma etch, CCl_4 pressure set to 50 mTorr, then 16 sccm N_2 added, shutter open, 30 W, 30 sec
S52	Plasma etch in 5 sccm CCl_2F_2 + 16 sccm N_2, shutter open, 30 W, 100 mTorr, 15 sec
S52C	Control experiment for S52 — no deposition performed after plasma etch
S53C	Control experiment for S53 — no deposition performed after plasma etch (performed before S53)
S53	Plasma etch in 5 sccm CCl_2F_2 + 16 sccm N_2, shutter open, 30 W, 100 mTorr, 2 min
S62	300°C; 2 min NH_4OH: 30% H_2O_2:H_2O (5:2:240) etch of non- lowed by deionized water rinse, cold platen, 15 sec plasma etch in flowing HCl, 200 W, maximum roughing pump throughput
S64	300°C; 2 min NH_4OH: 30% H_2O_2:H_2 (5:2:240) etch of non- anodized sample followed by deionized water rinse, cold platen, gas flows at start of deposition 16 sccm N_2 + 90 sccm SiH_4 + HCl (controlled by uncalibrated needle valve), HCl flow terminated immediately after turning on rf for deposition

SECTION 4

ANNEALING BEHAVIOR OF SILICON NITRIDE LAYERS PRODUCED BY PLASMA ENHANCED DEPOSITION

During the last semester of this program, we performed an exploratory study of the effects of post-deposition thermal annealing on the interfacial properties of PED silicon nitride films with n-GaAs substrates. Samples from four PED runs (S62 through S65, inclusive) were annealed for 30 min in N_2 at 400°C, 500°C, and 600°C. The wet-chemical treatment of the substrates was identical for all four runs. Fresh substrates were solvent and HCl-cleaned using our standard procedure (Table 2), etched 2 min in NH_4OH: 30% H_2O_2:H_2O (5:2:240), rinsed in deionized water, and placed onto a cold platen in the deposition chamber. In run S62, the sample was plasma etched using HCl, as summarized in Table 6. Electrical characteristics of an unannealed MIS capacitor incorporating a dielectric from run S62 are presented in Figure 8. For run S63, the sample surface was exposed to an H_2 preburn, as summarized in Table 4. Electrical characteristics of an unannealed MIS capacitor employing a dielectric from run S63 are presented in Figure 10. Run S64 was performed in a manner yielding HCl "doped" films, as summarized in Table 6. The capacitance-voltage and conductance-voltage characteristics of an unannealed MIS capacitor prepared from a sample produced in run S64 are illustrated in Figure 9. Run S65 was identical to run S63 except that a liquid-phase epitaxial layer (LPE 1552-III, $n \sim 10^{16}$ cm^{-3} on an n^+ Te-doped substrate) was included, along with an unintentionally doped n-type wafer of the type we normally used for each run.

We observed that annealing improved the C(V) and G(V) characteristics of samples from each run. However, the best results were obtained from run S63. C(V) and G(V) data for run S63 for 400°C, 500°C, and 600°C anneals are shown in Figures 11 through 13, respectively. The improvement can be seen by the reduction of capacitance frequency dispersion for accumulation bias and by the narrowing and lowering of the G(V) peak for each frequency. Note also that as the anneal temperature increases, the capacitance-voltage curve for each frequency shifts toward more negative gate voltages. This behavior indicates a shift of the built-in surface potential toward flat band.

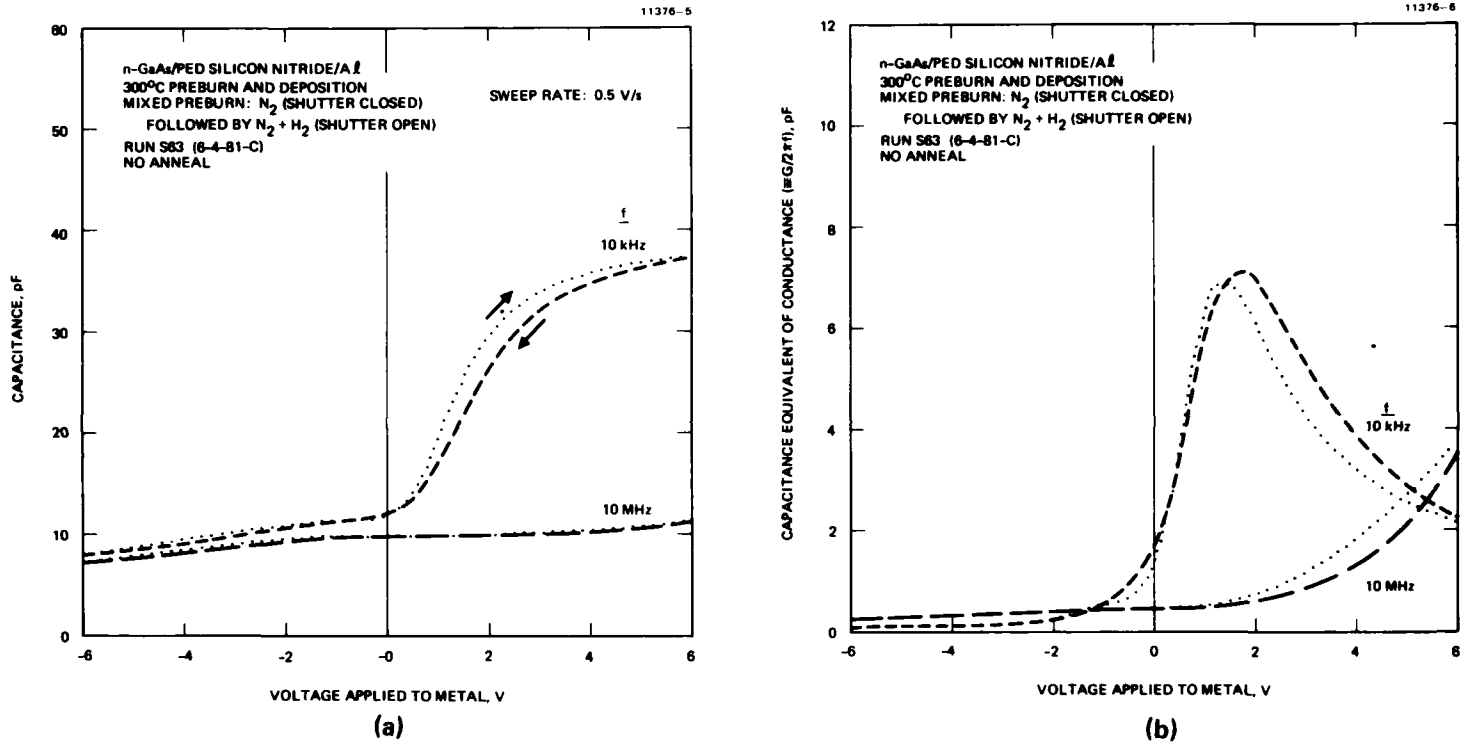

Figure 10. Electrical characteristics of an n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited at 300°C after exposure of the sample surface to an $N_2 + H_2$ preburn.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

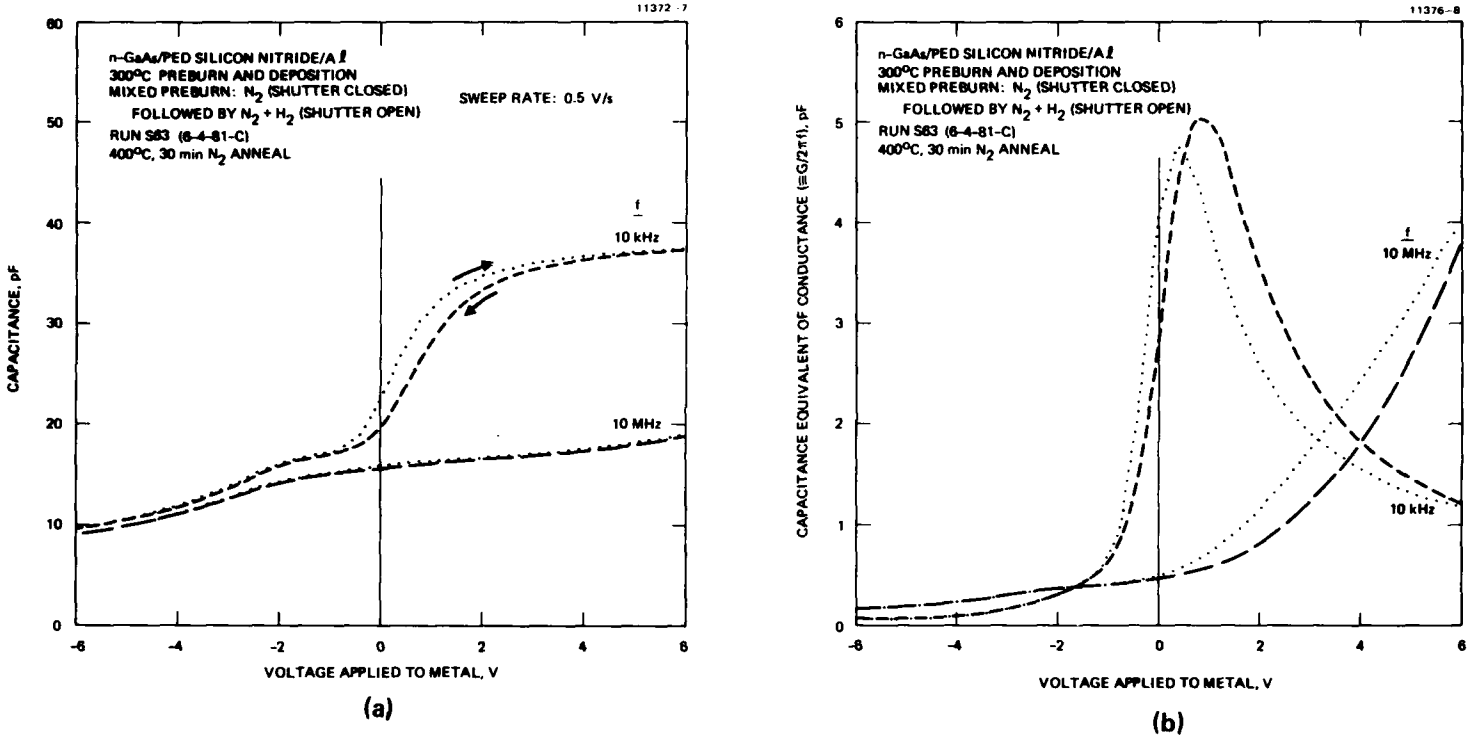

Figure 11. Electrical characteristics of an n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric from the same run as the sample of Figure 10 annealed at 400°C in nitrogen for 30 min prior to metal deposition.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

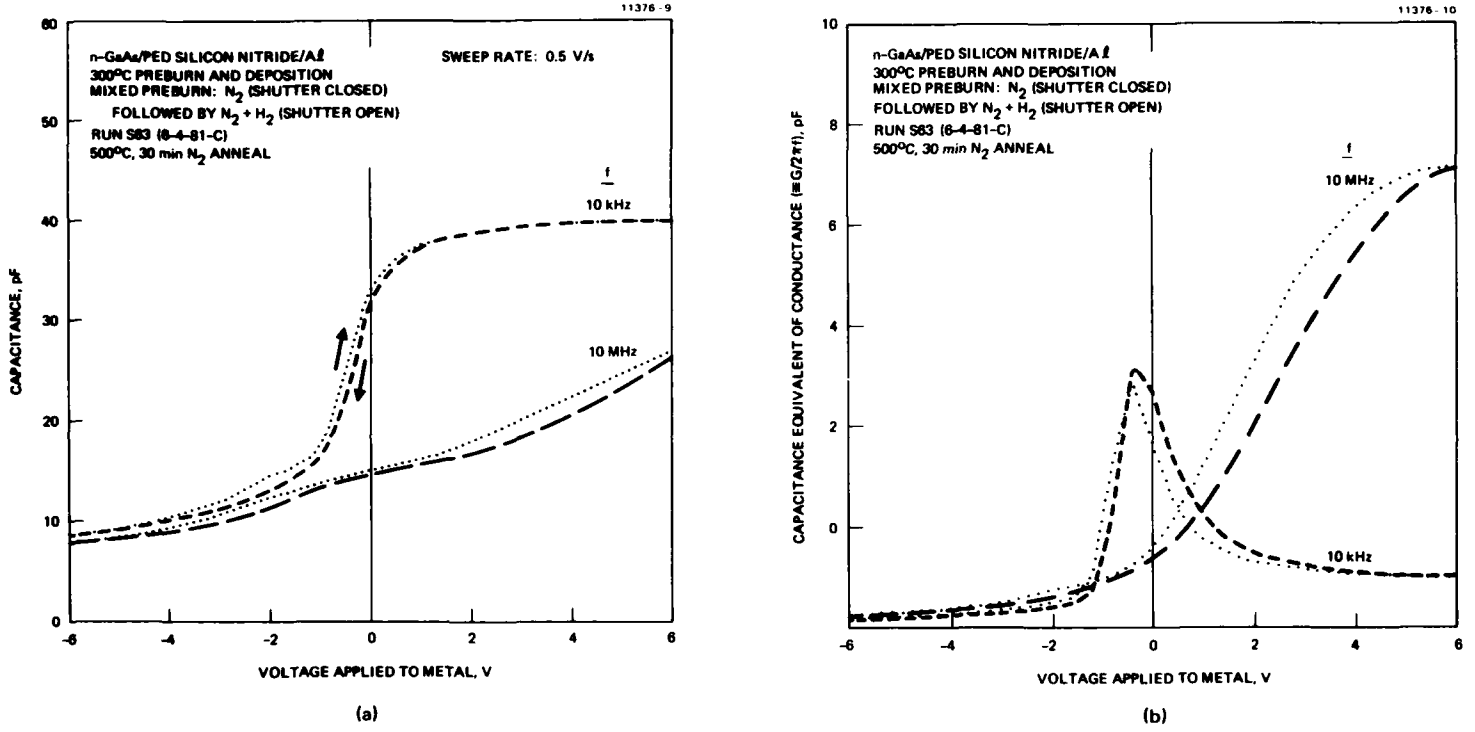

Figure 12. Electrical characteristics of an n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric from the same run as the sample of Figure 10 annealed at 500°C in nitrogen for 30 min prior to metal deposition.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

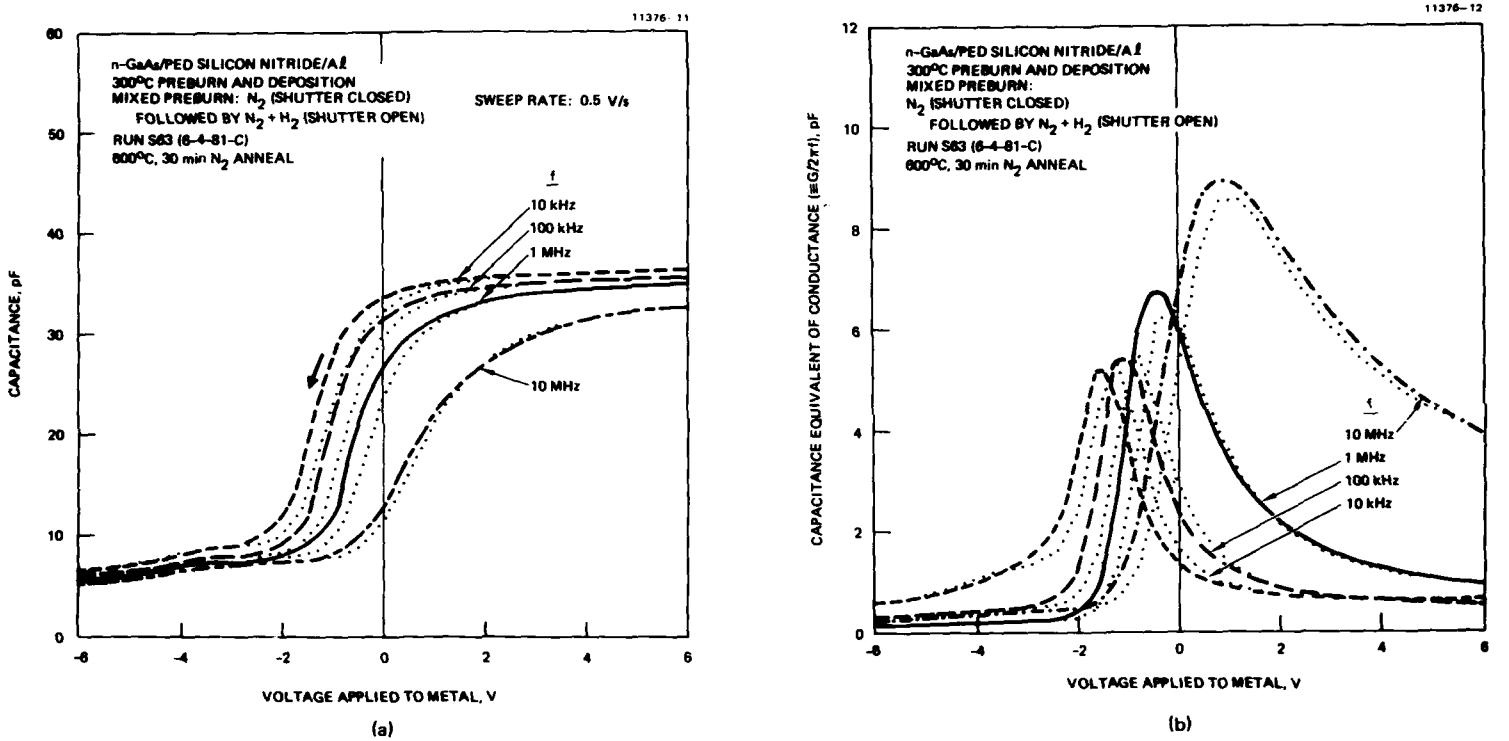

Figure 13. Electrical characteristics of an n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric from the same run as the sample of Figure 10 annealed at 600°C in nitrogen for 30 min prior to metal deposition.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

In view of these encouraging results, we chose to examine reproducibility with different substrate material as well as to further investigate annealing. Run S65 was nominally identical to run S63 except that two different substrate materials were used, as indicated above. Each substrate from run S65 was cleaved into four pieces which were isothermally annealed at 600°C in N_2 for times of 2 min, 10 min, 30 min, and 60 min. The best C(V) characteristics, shown in Figure 14 for the LPE material, were obtained for the 60 min anneal. Comparable results were observed for the bulk crystal substrate. Comparison of Figures 13 and 14 shows that, aside from differences likely attributable to different substrate doping, runs S63 and S65 gave very similar C(V) characteristics.

These results indicate that a post-deposition anneal is probably essential for best interface properties with PED SiN_x, particularly if the deposition temperature is well below 600°C. With annealing included in the process, the effects of different in situ substrate treatments become quite evident. For example, Figures 15(a) and 15(b) illustrate the C(V) and G(V) characteristics, respectively, of a sample from run S62 (in which the sample surface was plasma etched in HCl prior to dielectric deposition) following annealing at 600°C for 30 min. Comparison of the data of Figure 15 with the characteristics shown in Figure 13 clearly indicates that the interfacial properties of the sample of Figure 13 (in which the sample was exposed to an $N_2 + H_2$ preburn) following annealing at 600°C are far superior to those of the sample of Figure 15.

At least two mechanisms may contribute to this interface improvement. A 600°C anneal is known to cause some restructuring of PED SiN_x, and some lattice damage in GaAs is removed at this temperature (e.g., the threshold for electrical activation of ion implanted Be is 550°C).

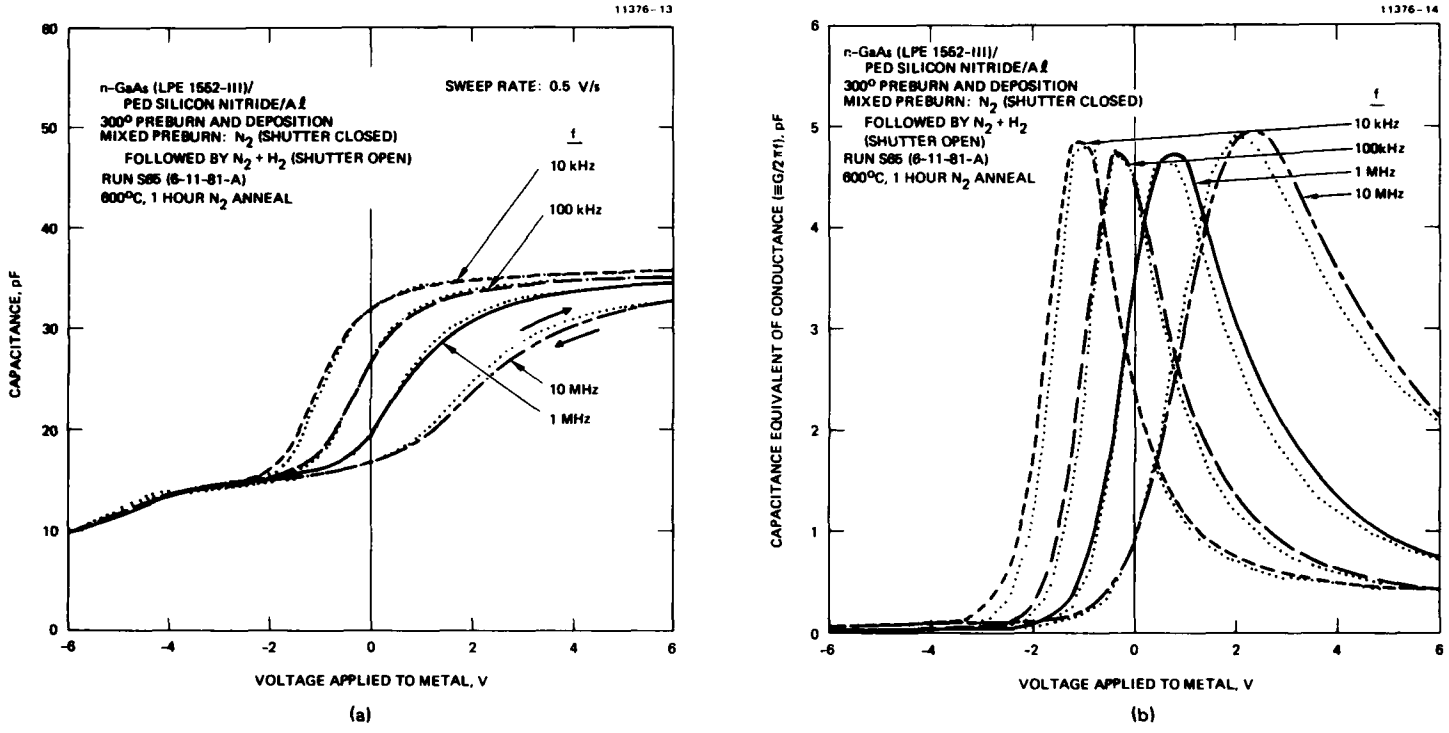

Figure 14. Electrical characteristics of a n-GaAs (LEPI 1552-III)/PED silicon nitride/Al capacitor incorporating a dielectric deposited at 300°C after exposure of the sample surface to an $N_2 + H_2$ preburn and annealed at 600°C for 1 hr in N_2 prior to Al deposition.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

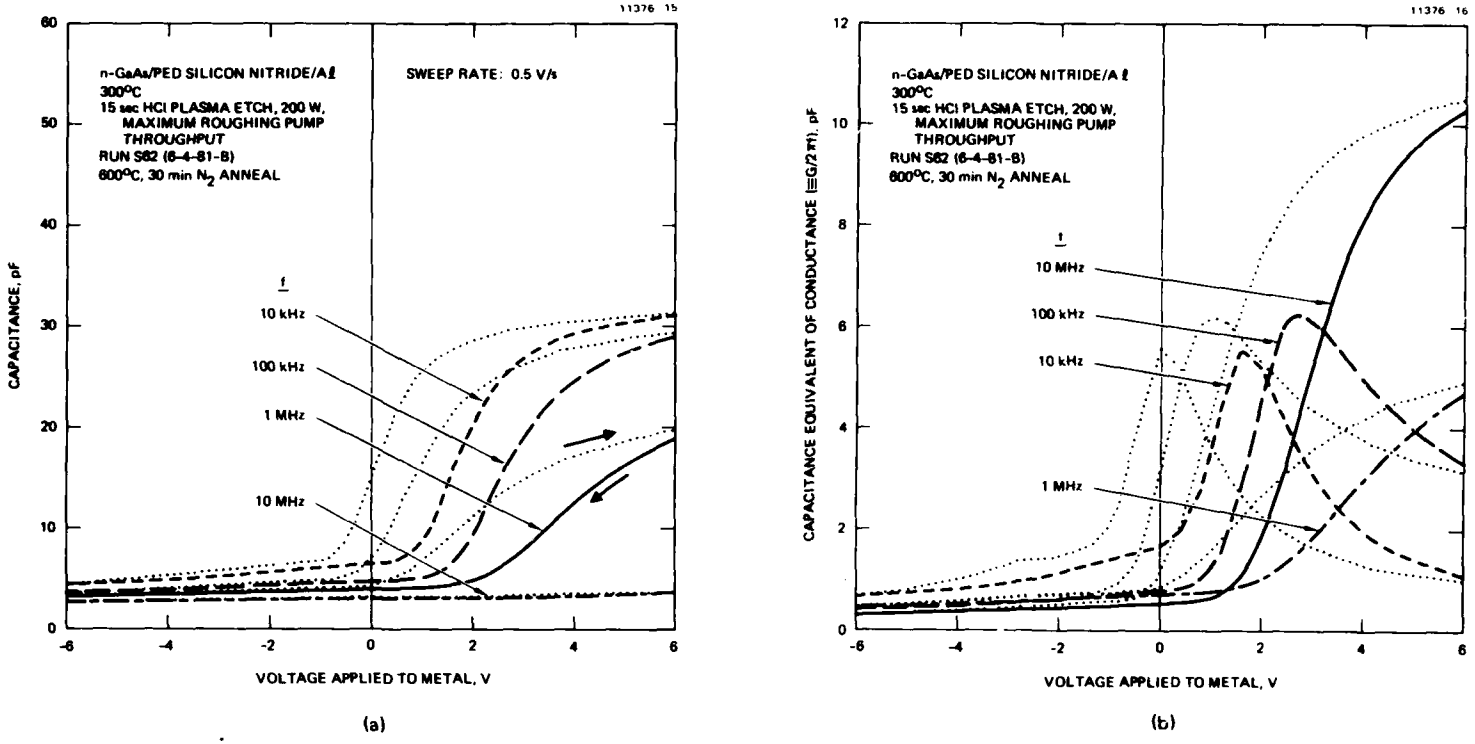

Figure 15. Electrical characteristics of a n-GaAs/PED silicon nitride/Al capacitor incorporating a dielectric deposited at 300°C after a 15 sec plasma etch of the sample surface in HCl and annealed for 30 min at 600°C in N_2 prior to metal deposition.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

SECTION 5

PYROLYTIC CHEMICAL VAPOR DEPOSITION OF SILICON NITRIDE

Pyrolytic chemical vapor deposition of dielectrics for this program was performed in the reactor shown in Figure 16. This unit is a helium leak-tight, highly interlocked system capable of growing a wide variety of oxides, nitrides, and oxy-nitrides with a high degree of composition control. It operates at ambient pressure. Sample heating is produced by rf heating of a graphite susceptor coated with silicon carbide. A feedback circuit permits very rapid variations of temperature to be produced controllably. This capability permits films to be deposited on GaAs at temperatures at which GaAs normally dissociates. For example, silicon nitride can be deposited very rapidly at 700°C. By ramping the sample temperature from 250°C to 700°C in 9 sec or less, silicon nitride films have been deposited on GaAs with no observable degradation of the GaAs surface.

In order to minimize the possibility of surface decomposition, pyrolytic silicon nitride depositions for this program were performed at the lowest practical temperature (615°C).

Gas flow rates employed were as follows:

- SiH_4: 11 sccm
- NH_3: 3.6 slm
- N_2 carrier: 29 slm.

At the deposition temperature of 615°C, the deposition rate of the film was about 20 nm/min. Prior to deposition, the gas flows were stabilized with the substrate held at 315°C. The sample temperature was then ramped to the deposition temperature in ~9 sec. This procedure minimizes thermal decomposition of the sample prior to the beginning of film deposition.

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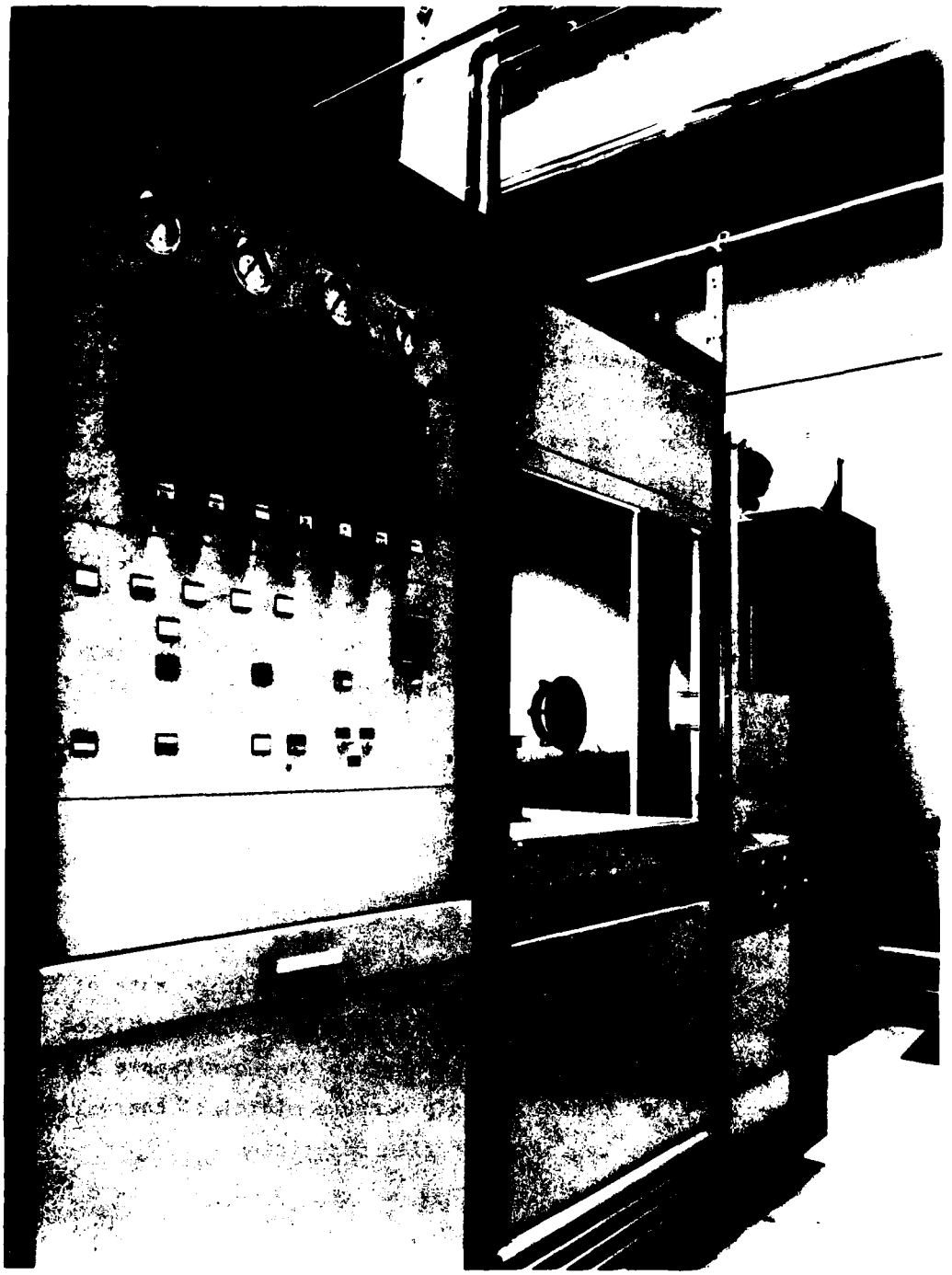


Figure 16. Pyrolytic chemical-vapor-deposition system.

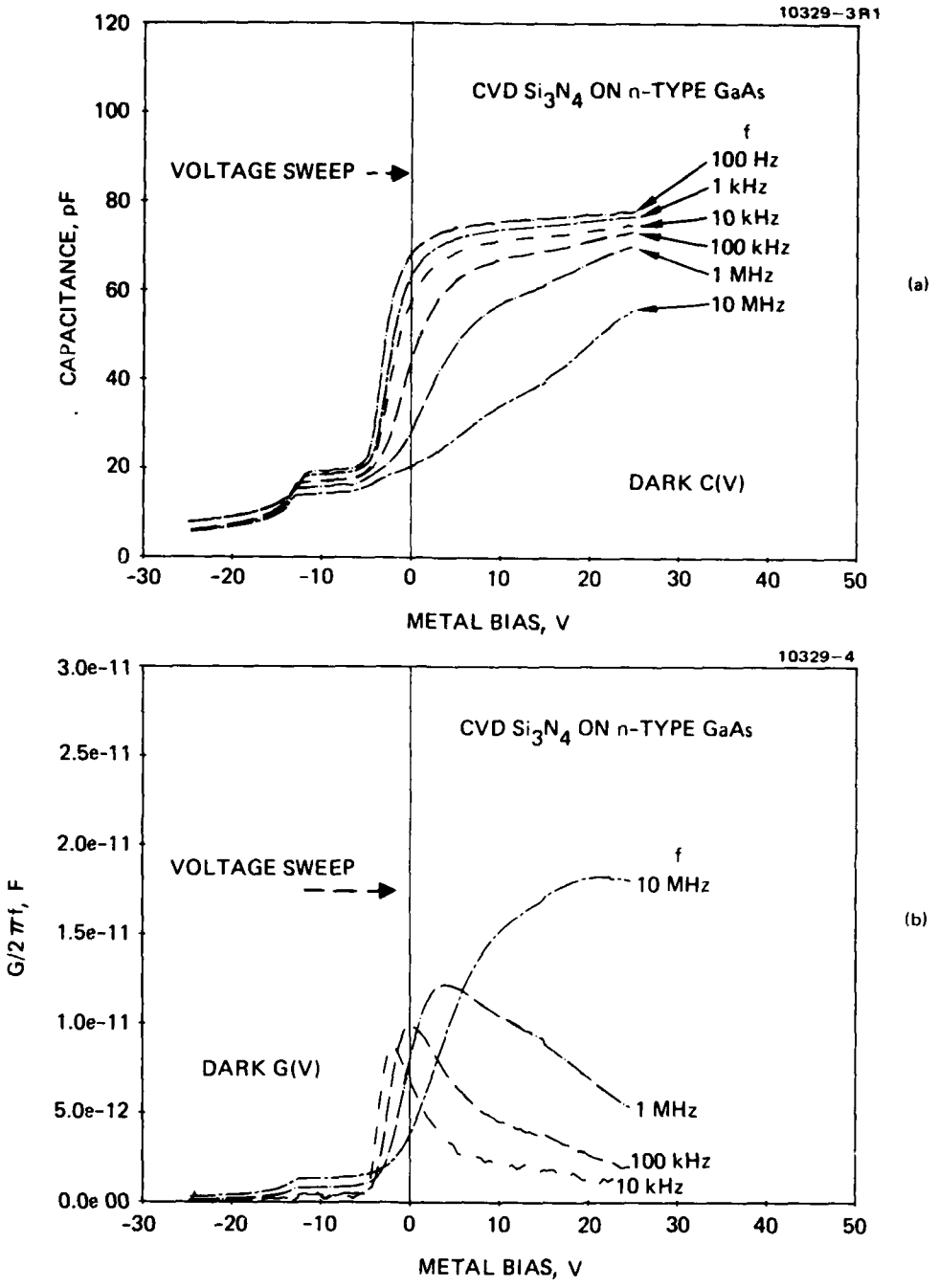


Figure 17. Electrical behavior of Al/CVD Si_3N_4/n-GaAs MIS capacitors in the dark.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

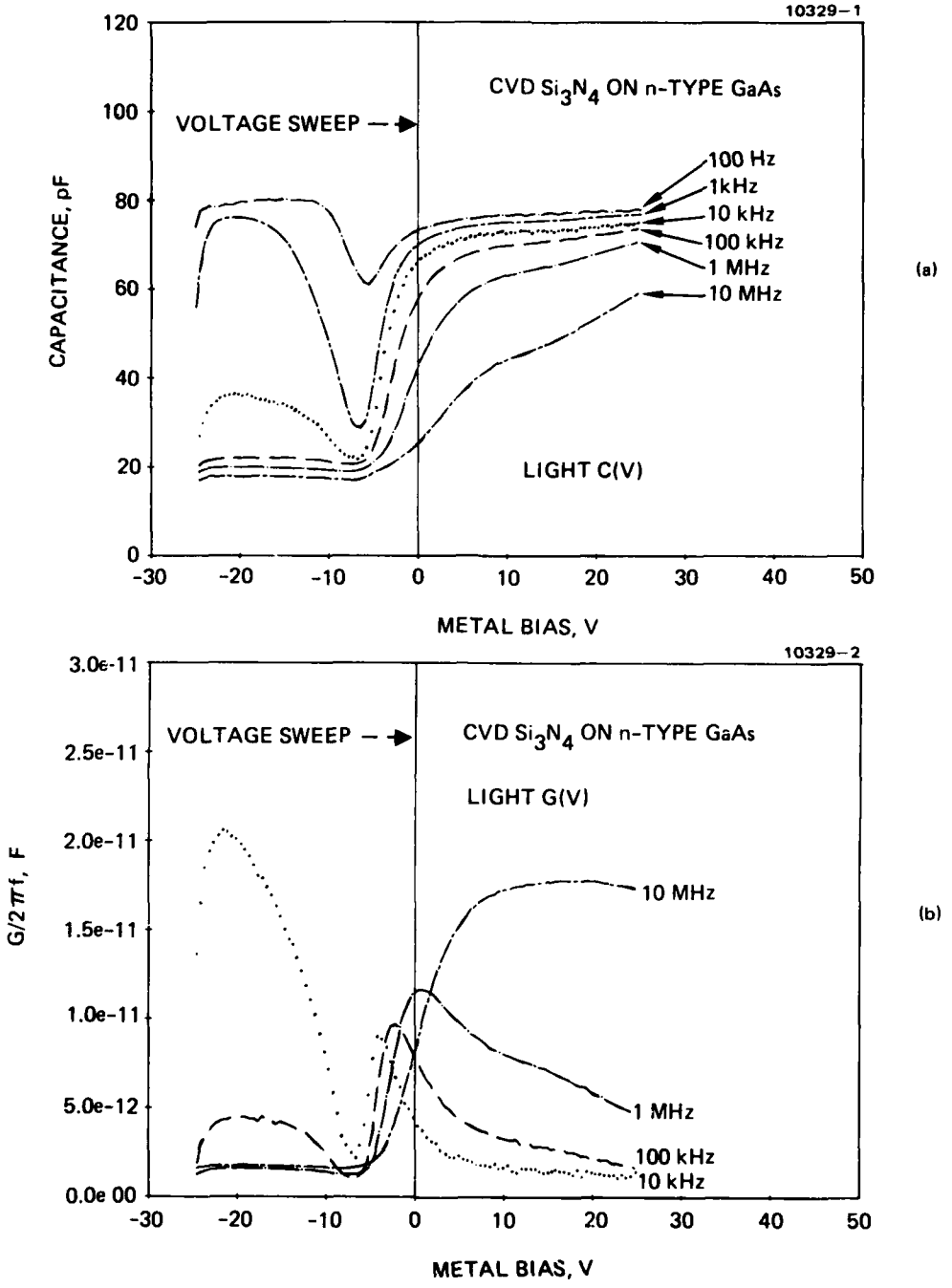


Figure 18. Electrical behavior of Al/CVD Si_3N_4/n-GaAs MIS capacitors under illumination.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

A. EVIDENCE FOR INVERSION OF THE n-TYPE GaAs SURFACE UNDER PYROLYTIC Si_3N_4

Capacitance-voltage and conductance-voltage data for an Si_3N_4 sample are shown in Figures 17(a) and 17(b), respectively. Ellipsometric parameters of the film were n = 1.95 and thickness = 47 nm. Capacitor structures were formed by depositing 0.29-mm-diameter, ~250-nm-thick Al dots. Substrate material was n-type with a nominal donor concentration of 1.7×10^{15} cm^{-3} and a mobility of 4900 $cm^2/V\text{-sec}$. The C(V) data of Figure 17(a) show substantial frequency dispersion for accumulation bias. The 10-MHz data evidently do not represent the high-frequency limit. For inversion bias, there are indications of possible pseudo-inversion behavior between -3 V and -10 V. A theoretical inversion capacitance C_{inv} of 7.3 pF was computed using the nominal donor concentration of the substrate and an insulator capacitance of 75 pF, which is the largest measured capacitance at 10 kHz. The pseudo-inversional level is substantially greater than C_{inv}. However, beyond -10 V, the capacitance actually drops slightly below C_{inv}, suggesting that a stable deep depletion condition may exist. To avoid a transient deep depletion, the sample was illuminated while biased at -20 V and the illumination was then removed for the voltage scan.

To further explore the properties of these capacitors in the deep depletion region, we measured the C(V) and G(V) characteristics of these samples under illumination. The results suggest that it might be possible to achieve a p-type inversion layer if a sufficiently high minority carrier generation rate is provided.

C-V behavior was measured from 100 Hz to 10 MHz for a device illuminated with light from a tungsten lamp filtered with a red Wratten No. 25 filter. The C(V) data are shown in Figure 18(a). G(V) data from 10 kHz to 10 MHz are shown in Figure 18(b). Conductance data for 100 Hz and 1 kHz were not recorded.

The rise in the low-frequency capacitance for negative bias is the most notable feature of Figure 18(a). The dark C-V and G-V data for this device are shown for comparison in Figure 17. We interpret the rise in capacitance as evidence for formation of a p-type inversion layer. Response of the inversion layer charge to the ac voltage is apparently enhanced by lateral diffusion of

photogenerated holes from the region around the capacitor electrode. Since the electrode is 250-nm-thick Al and is thus opaque, photogeneration directly under the electrode is precluded.

The low frequency capacitance under illumination decreased again for bias less than -20 V. A possible mechanism for this behavior is a depletion of inversion charge by conduction through the dielectric in competition with the indiffusion of photogenerated holes. Evidence supporting this hypothesis is provided by the illuminated and dark dc current density versus voltage (J-V) data shown in Figure 19. Substantial photocurrent is observed only for negative metal bias that corresponds to inversion. Furthermore, the illuminated J(V) curves of Figure 19(b) exhibit saturation beyond 20 V with a saturation current density that increases with light intensity. Since the steady-state concentration of holes, and hence the lateral hole diffusion current, increases with light intensity, the photocurrent saturation behavior is consistent with the hypothesis.

Removal of inversion charge by dielectric leakage also explains stable deep depletion behavior under inversion bias, as can be seen in Figure 17(a), and has been observed for other samples. The ideal high-frequency inversion capacitance is independent of bias for a sufficiently low bias sweep rate. Just such behavior is seen in the 100 kHz, 1 MHz, and 10 MHz data of Figure 18(a), where the capacitance saturates at ~20 pF. However, for the dark C-V data of Figure 17(a), the capacitance first saturates at roughly 20 pF for increasing inversion bias and then, beyond ~ -12 V, decreases further. Note that -12 V corresponds approximately to the voltage at which the light and dark J-V curves of Figure 19(b) substantially diverge. Thus, deep depletion occurs when dielectric leakage of minority carriers surpasses the rate of thermal generation. The additional supply of minority carriers by photogeneration allows ideal high-frequency inversion behavior to be maintained to a greater bias voltage.

These results demonstrate that dielectric leakage must be considered when interpreting GaAs MIS C-V data. Compared to Si MOS with thermal SiO_2, we may expect higher leakage currents with deposited dielectrics and lower generation rates because of the greater bandgap energy of GaAs.

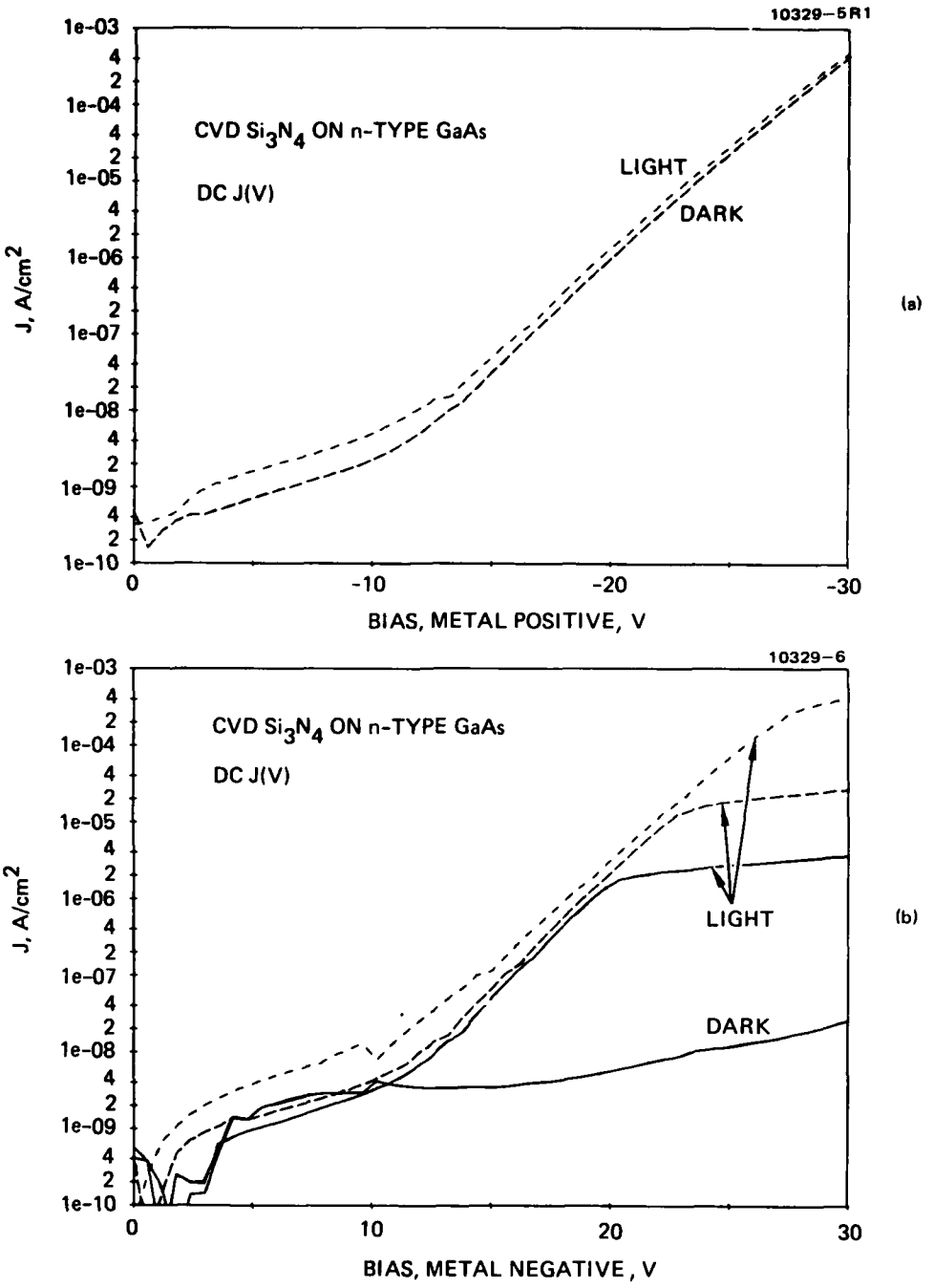


Figure 19. Current density versus voltage behavior of Al/CVD Si_3N_4/n-GaAs MIS capacitors.
(a) Accumulation regime
(b) Depletion regime

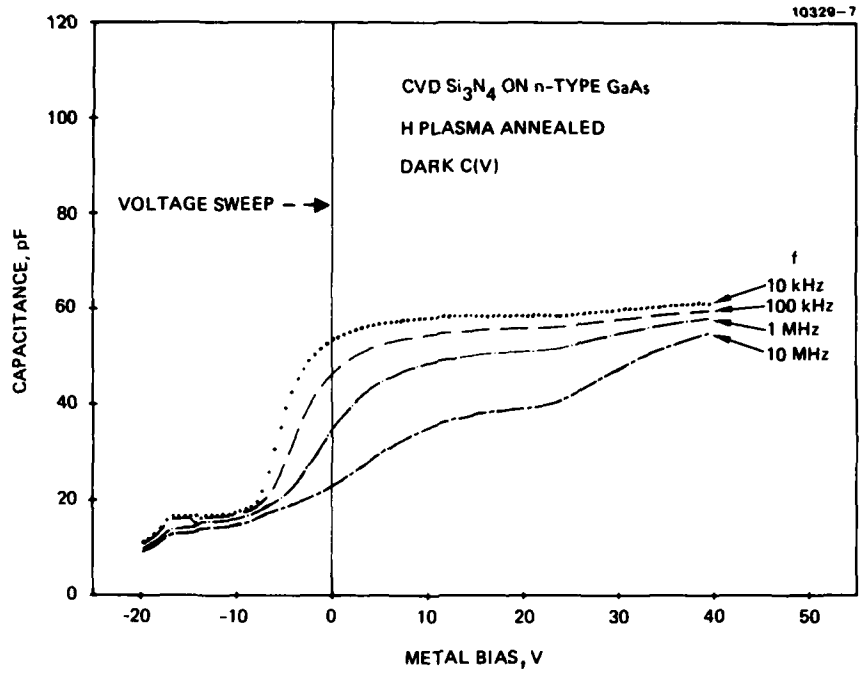


Figure 20(a). C-V behavior of Al/H-Annealed CVD Si_3N_4/n-GaAs MIS capacitors.

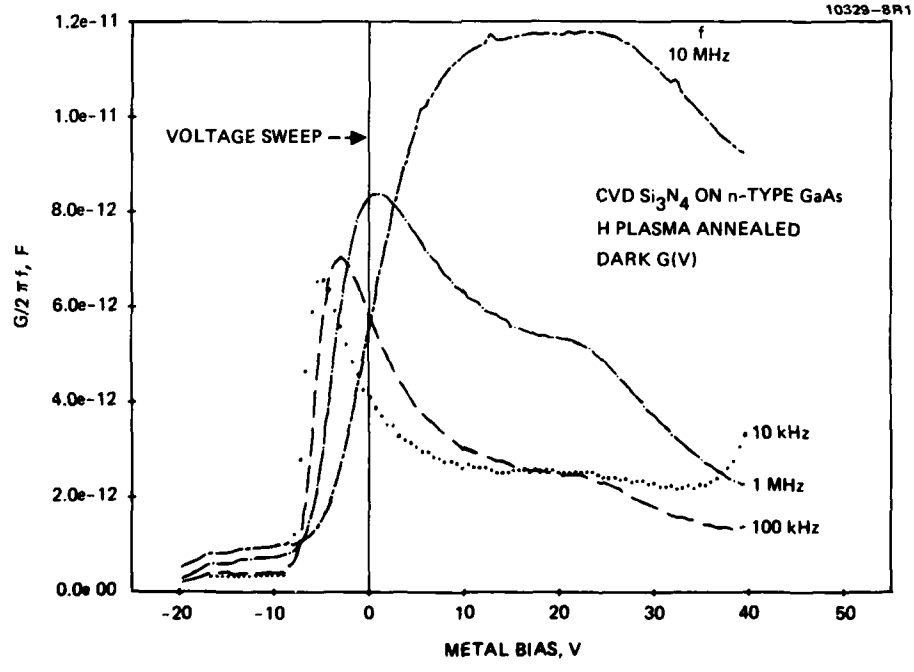


Figure 20(b). G-V behavior of Al/H-Annealed CVD Si_3N_4/n-GaAs MIS capacitors.

B. HYDROGEN PLASMA ANNEALING OF PYROLYTIC Si_3N_4

In an attempt to improve the interface electrical properties of pyrolytic Si_3N_4 on GaAs, we investigated the effect of a hydrogen plasma anneal on the passivating behavior of the material. This approach was suggested by published reports on improvement of the electrical and optical properties of poly-Si produced by H plasma annealing. The effect on poly-Si is thought to be due to hydrogenation reducing the number of deep localized states.

The plasma anneal was performed in our modified LFE PND-301 reactor under the following conditions:

Temperature	300°C
Feed gas	H_2
Chamber pressure	1 Torr
RF power	250 W
Anneal time	30 min.

After annealing, MIS capacitors were formed by applying 0.29-mm-diameter Al electrodes and backside ohmic contacts.

The measured C-V and G-V data are shown in Figures 20(a) and 20(b), respectively. Comparing these data with data for unannealed samples, no improvement due to the H plasma anneal is readily evident. Consequently, we terminated studies of this procedure.

C. IN SITU PYROCHEMICAL TREATMENTS OF THE GaAs SURFACE

During the last six months of this program, nine deposition runs were performed to assess the effects of in situ pyrochemical treatment of the GaAs surface prior to deposition on the electrical properties of the Si_3N_4/GaAs interface. Before insertion into the deposition chamber, substrates were cleaned by baseline technique described in Section 2. The pyrochemical treatment consisted of heating the substrate to a predeposition temperature in the range of 450 to 550°C for a selected "soak time" of 5 or 10 min, after which the temperature was increased rapidly to the deposition temperature and deposition initiated by introduction of SiH_4.

For five of these runs, the predeposition ambient was $NH_3 + N_2$ at respective flow rates as used for deposition, and temperature varied from 450°C to 550°C. Two runs employed a N_2 predeposition ambient, at temperatures of 450°c and 550°C. Two runs employed a N_2 predeposition ambient, at temperatures of 450°C and 500°C, with NH_3 being introduced simultaneously with SiH_4 to start deposition.

Capacitance-voltage data on these samples indicates strong pinning of the surface potential and interface properties substantially inferior to the best results with PED SiN_x.

SECTION 6

PLASMA ENHANCED DEPOSITION OF GERMANIUM NITRIDE AND SILICON NITRIDE/GERMANIUM NITRIDE MIXTURES

Twelve runs were performed to identify deposition parameters suitable for preparing germanium nitride films with acceptable dielectric properties by plasma-enhanced deposition (PED), and four runs were performed to establish preliminary parameters for the deposition of Si_3N_4/Ge_3N_4 mixtures.

A. DEPOSITION OF GERMANIUM NITRIDE FROM GERMANE AND NITROGEN

A baseline process for the deposition of PED germanium nitride was established early in the fifth semester of the program. Deposition parameters giving films with an index of refraction expected for Ge_3N_4 were initially determined by ellipsometry. A film about 50 nm thick was then deposited on pyrolytic carbon and analyzed by Rutherford backscattering (RBS). The RBS spectrum was interpreted as showing no oxygen contamination. However, because of problems with the RBS system that prevented normal plotting of the data, determination of the Ge/N ratio from these data was not attempted. The GeN_x deposition parameters established as base line are as follows:

Nitrogen plasma preburn:

Shutter: Closed

Temperature: 200°C

N_2 flow rate: 16 sccm

System pressure: 100 mTorr

RF power: 100 W

Duration: 10 min

Deposition:

Temperature: 200°C

Hot plate rotation: on (6 rpm)

N_2 flow rate: 16 sccm

Flow rate of 1.5% GeH_4 in Ar: 80 sccm

Germane dispersal ring motion: on (passes over hot plate 6 times per minute)

System pressure: 250 mTorr

RF power: 50 W

Deposition rate: ~9 nm/min

Deposition time: 10 min.

All other procedures employed were identical to the baseline silicon nitride process described in Section 2.C. Four deposition runs were performed using the germane/nitrogen process. One run, G1, was performed using the baseline process. This run yielded films with an index of refraction of 1.92. MIS capacitors incorporating the baseline germanium nitride films exhibited large frequency dispersion under accumulation bias similar to that observed for PED silicon nitride films. In addition, the germanium nitride films exhibited an irreversible decrease in capacitance when the applied field exceeded $\sim 10^6$ V cm^{-1}.

The remaining three germanium nitride runs using the germane/nitrogen were performed without a second pumpdown to high vacuum after the preburn stage (similar to the revised standard PED silicon nitride procedure). In run G2, the sample was loaded onto a cold platen and no preburn was performed. For run G3, the sample was loaded onto a cold platen and the preburn was performed with the shutter open. Run G4 was performed at 300°C after the sample was loaded onto a cold platen, heated to 300°C after pumpdown to high vacuum, and no preburn

performed. Samples from all three runs exhibited high conductance values with frequency and bias dependence indicative of high insulator leakage current.

Some reasonably well-behaved capacitors were obtained from run G3. The electrical characteristics of one such capacitor are presented in Figures 21(a) and 21(b). Note that the voltage scale of Figures 21(a) and 21(b) differ from that of Figures 3 through 9 because of the relatively low fields which could be applied to the germanium nitride films without altering their electrical properties. Over this limited range of fields, the frequency dispersion of the accumulation capacitance of the sample of Figure 21 is definitely inferior to our best results obtained with PED silicon nitride dielectrics, but is comparable to some of our earlier results (e.g., those shown in Figure 4(a)). The conductance behavior of this sample between 100 kHz and 10 MHz is also similar to the data of Figure 4(b). The 10 kHz conductance of the germanium nitride sample behaves very differently from that of the silicon nitride films because of the relatively high leakage of the germanium nitride films at low frequencies.

Subsequent to these experiments, it was discovered that the performance of the Rutherford backscattering (RBS) system used to analyze the oxygen content of the baseline germanium nitride films was impaired by partial failure of the data display system. The films were not, in fact, oxygen-free. New RBS data taken after correction of the display problem indicate this material has an O:N ratio of about 3:2.

B. INVESTIGATION OF PLASMA ENHANCED DEPOSITION OF GERMANIUM NITRIDE FROM GERMANE AND AMMONIA

During the last semester of this contract, we attempted to prepare PED germanium nitride films with improved composition and interface electrical properties by reaction of germane and ammonia. The baseline procedure for this process follows the same steps as the revised standard process for PED silicon nitride deposition but differs from it in the gases and conditions employed for the preburn and deposition steps. The parameters for these steps are as follows:

Ammonia plasma preburn:

Shutter: Open

Temperature: 250°C

Hot Plate position: lowest

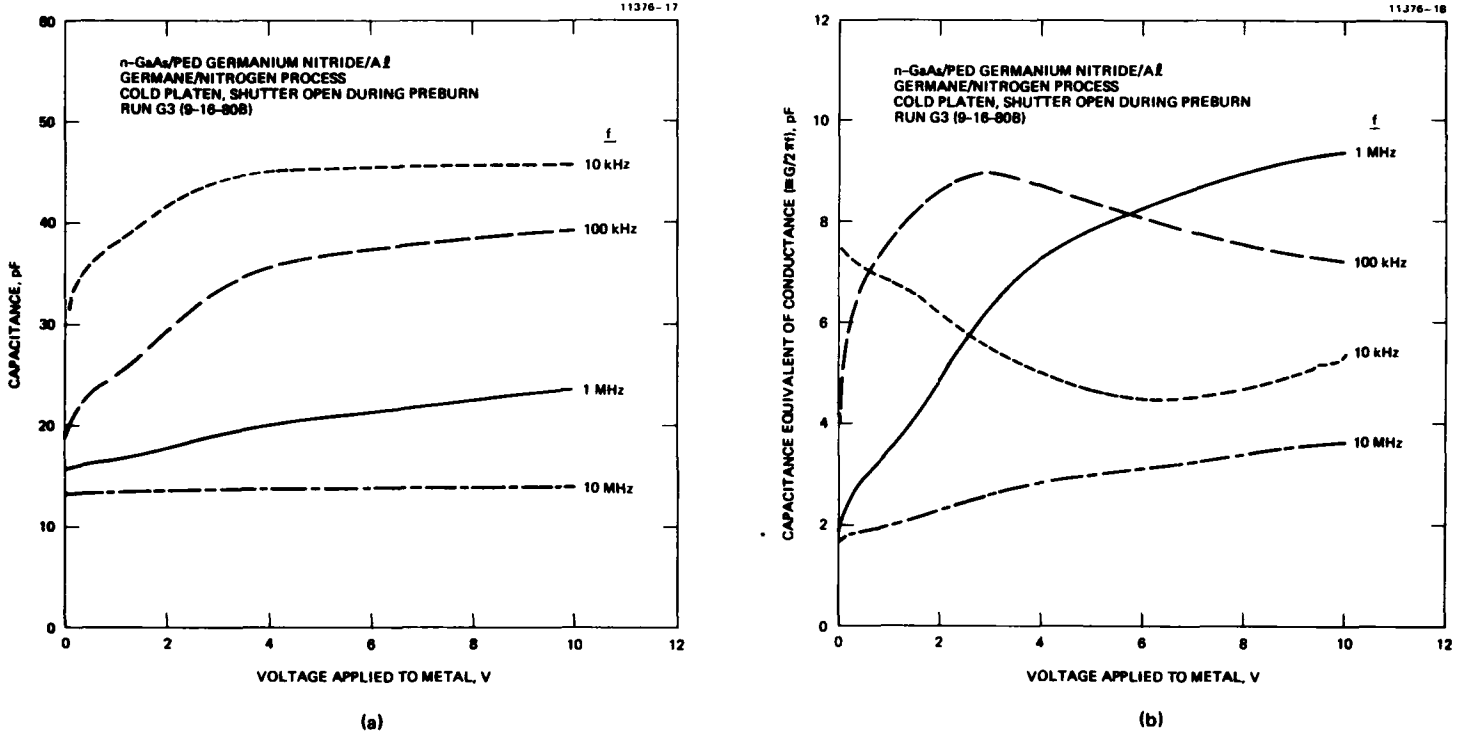


Figure 21. Characteristics of a n-GaAs/PED germanium nitride/Al capacitor employing a dielectric prepared by the germane/nitrogen process with the sample loaded on a cold platen and the shuttle open during the N_2 preburn.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

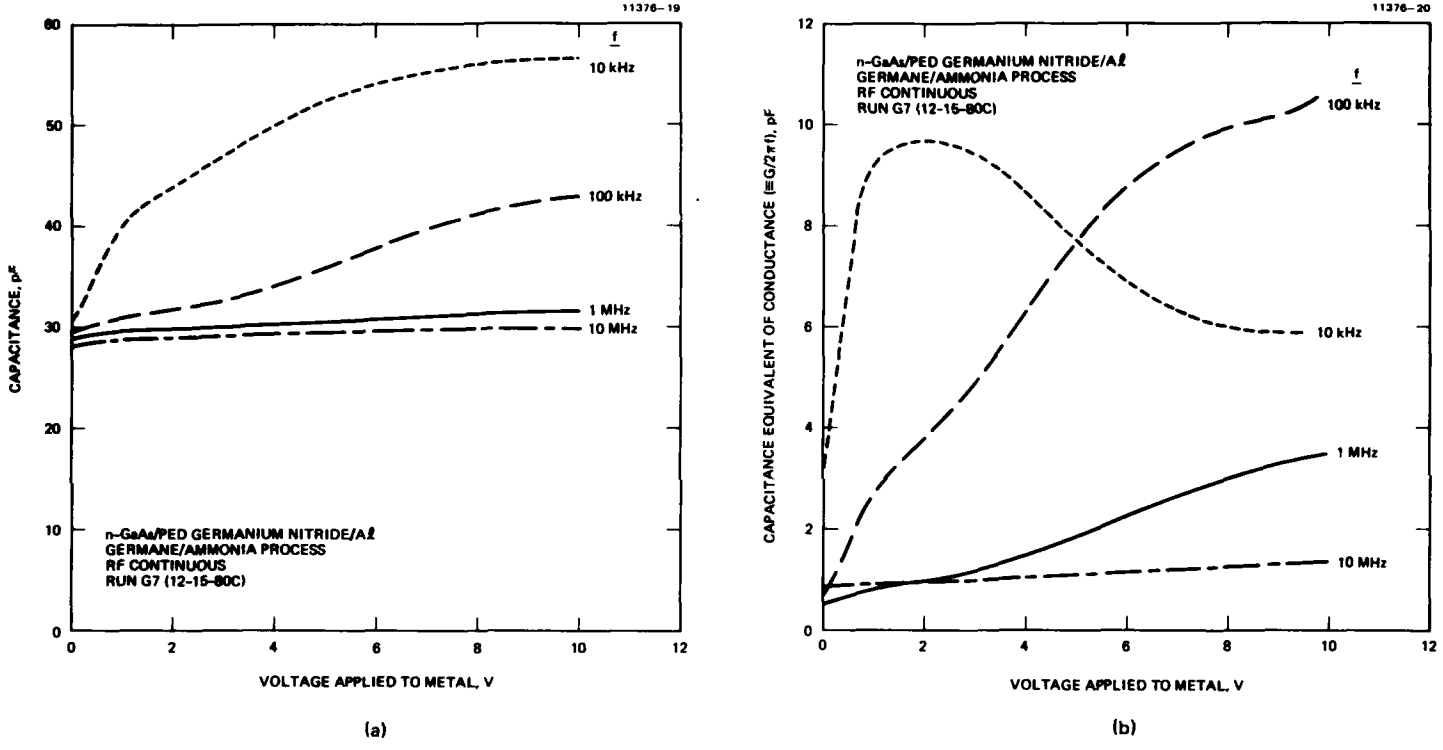


Figure 22. Characteristics of a n-GaAs/PED germanium nitride/Al capacitor employing a dielectric prepared by the germane/ammonia process with the rf power left on during the turn-on of the germane following the preburn.
(a) Capacitance-voltage characteristics
(b) Conductance voltage characteristics

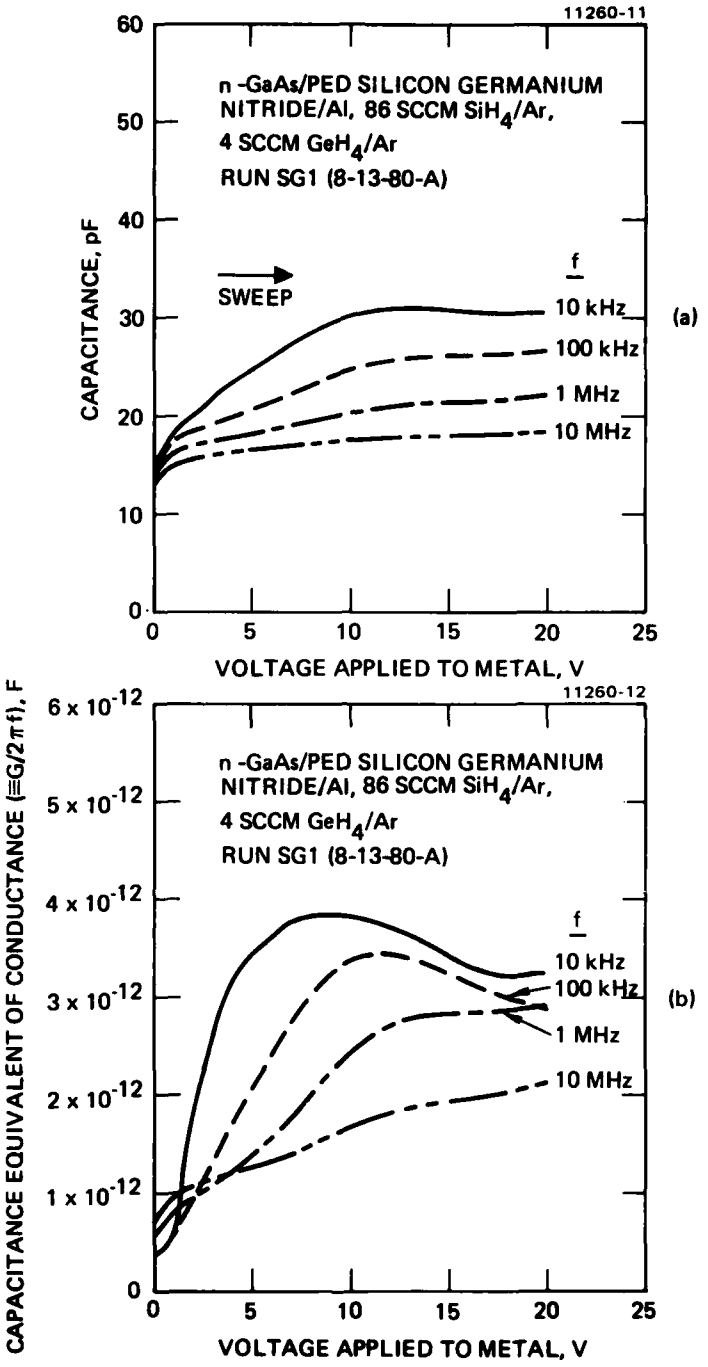


Figure 23. Characteristics of a n-GaAs/PED silicon germanium nitride/Al capacitor deposited with gas flows of 16 sccm N_2, 86 sccm of 1.5% SiH_4 in Ar, and 4 sccm of 1.5% GeH_4 in Ar.
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

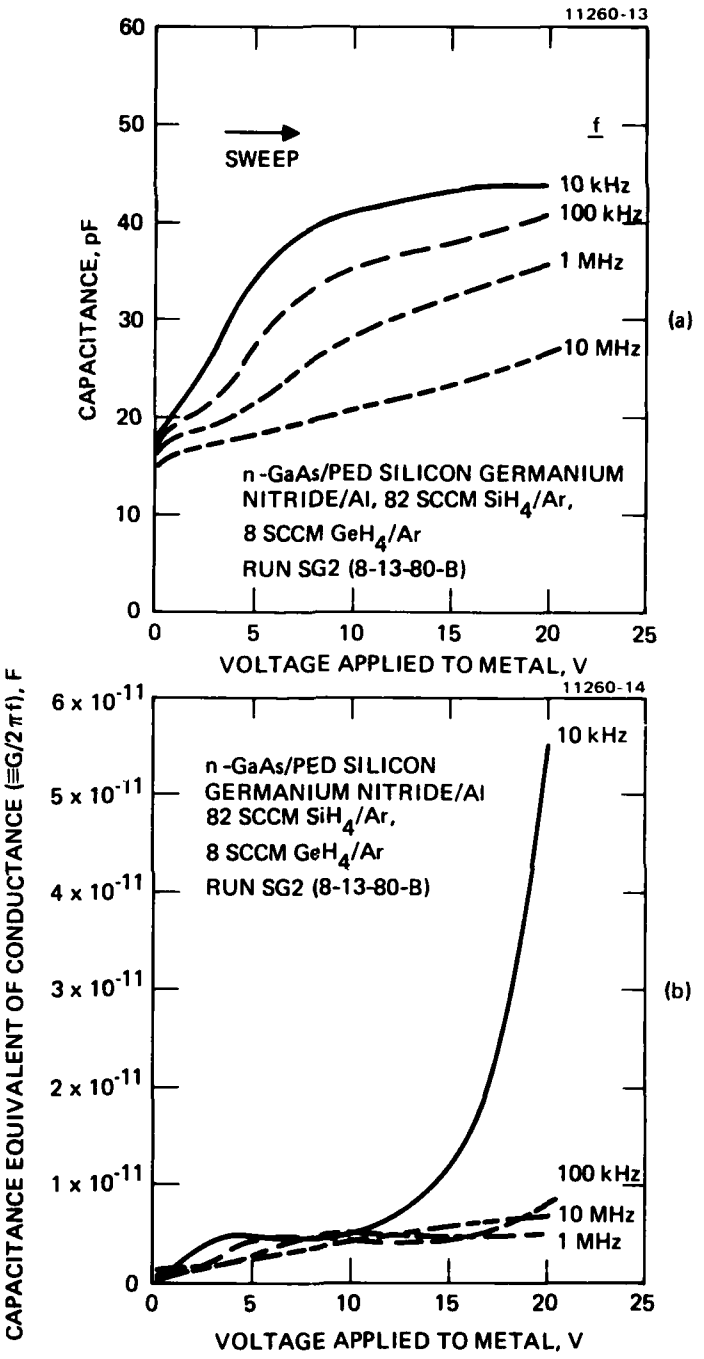


Figure 24. Characteristics of a n-GaAs/PED silicon germanium nitride/Al capacitor deposited with gas flows of 16 sccm N_2, 82 sccm of 1.5% SiH_4 in Ar, and 8 sccm of 1.5% GeH_4 in Ar
(a) Capacitance-voltage characteristics
(b) Conductance-voltage characteristics

Hot plate rotation: on (6 rpm)

NH_3 flow rate: 18 sccm

System pressure: 35 to 50 mTorr (5 to 7 Pa)

RF power: 20 W

Duration: 10 min

Deposition:

Temperature: 250°C

Hot plate position: Lowest

Hot plate rotation: on (6 rpm)

NH_3 flow rate: 18 sccm

Flowrate of 1.5% GeH_4 in Ar: 60 sccm

Germane dispersal ring motion: on (passes over hot plate 6 times per minute)

System pressure: 145 to 160 mTorr (19 to 21 Pa)

RF power: 20 W

Deposition rate: 3.1 nm/min

Deposition time: 24 min.

In the parameter list above, hot plate position refers to the vertical position of the rotating hot plate relative to the silane and germane dispersal

ring. In the lowest position, used for all the PED depositions of germanium nitride from germane and ammonia, the sample surface is roughly 10 cm below the dispersal ring. In the highest position, employed in all other PED depositions discussed in this report, the sample surface is approximately 2.5 cm below the dispersal ring.

A total of eight deposition runs were performed during the last semester of the program to explore the effects of process variations on the electrical properties of PED germanium nitride films prepared using the germane/ammonia process. The deviations of these runs from the baseline process are summarized in Table 7.

TABLE 7. Deposition Conditions for Germanium Nitride Runs Employing Germane and Ammonia as Reagents

Run	Deviation from Baseline Process Employing Germane and Ammonia
G5	Standard run
G6	10 min preburn, shutter closed, in 16 sccm N_2, 100 W, 100 mTorr
G7	RF power not extinguished between preburn and deposition
G8	5 min NH_4OH: 30% H_2O_2:H_2O (5:2:240) oxide strip, rf power not extinguished between preburn and deposition
G9	Repeat of G8
G10	Repeat of G8
G11	10 min preburn, shutter closed, in 16 sccm N_2, 200 W, 100 mTorr, followed by 10 min preburn, shutter open, in 18 sccm NH_3, 20 W, 42 mTorr, rf power not extinguished between preburn and deposition
G12	5 min NH_4OH: 30% H_2O_2:H_2O (5:2:240) oxide strip followed by methanol dip, cold platen, rf power not extinguished between preburn and deposition

Films prepared by the baseline germane/ammonia process exhibit refractive indices of roughly 1.96 and O:N ratios (determined by Rutherford backscattering) of about 3:4, which should be compared to a ratio of about 3:2 obtained by our baseline germane/nitrogen process. Thus the oxygen content of the films has been substantially reduced but not eliminated by employing the germane/ammonia technique.

All MIS capacitors formed on GaAs substrates using dielectrics from this series exhibited substantial frequency dispersion of the accumulation capacitance and poor conductance-voltage behavior. The most promising data were obtained from the baseline run, G5, and from run G7, in which the rf power was kept on continuously through the preburn and deposition stages. Capacitance-voltage and conductance-voltage data from an Al/PED germanium nitride/n-GaAs capacitor incorporating a dielectric film prepared in run G7 are shown in Figure 22(a) and 22(b), respectively. Comparison of the data of Figure 22 with that of Figure 21, from a germanium nitride/GaAs sample incorporating a dielectric prepared by the germane/nitrogen process, reveals that the electrical properties of the interface between the germane/ammonia process film and GaAs are somewhat inferior to those obtained with the germane/nitrogen film.

C. DEPOSITION OF SILICON GERMANIUM NITRIDE FROM SILANE, GERMANE, AND NITROGEN

The four runs attempting deposition of silicon nitride/germanium nitride mixtures were performed using revised standard silicon nitride process with the following exceptions: for run SG1, the sample was dipped into methanol after the standard oxide strip, loaded onto a cold platen wet, and heated to 200°C after pumpdown to high vacuum. The deposition was performed with gas flows of 16 sccm N_2, 86 sccm of 1.5% SiH_4 in Ar and 4 sccm of 1.5% GeH_4 in Ar; for run SG2, the same procedures as in run SG were employed, and the gas flows were 16 sccm N_2, 82 sccm of dilute SiH_4 and 8 sccm of dilute GeH_4. Runs SG3 and SG4 were performed at 300°C with no preburn, using gas flows identical to those of run SG1 for the deposition stage. For run SG4 the sample was loaded onto a cold platen. Run SG1 yielded films with an index of refraction of 1.89 and a thickness of 101 nm. Corresponding values from run SG2 were 2.05 and 87 nm.

Electrical characteristics of MIS capacitors incorporating dielectric films from runs SG1 (low Ge content, 200°C deposition), SG2 (high Ge content, 200°C), and SG3 (low Ge content, 300°C) are presented in Figures 23(a) and 23(b), 24(a) and 24(b), and 25(a) and 25(b), respectively. Comparison of Figures 23(a) and 23(b) with Figures 3(a) and 3(b) indicates that the film with low Ge content exhibits interfacial electrical properties somewhat inferior to the baseline PED silicon nitride film. The conductance for the silicon germanium nitride film does not peak at 1 MHz and the peaks for 10 kHz and 100 kHz for this film are very broad and occur at higher voltages than do those for Si_3N_4 film. The silicon germanium nitride sample also exhibits a shoulder in the 1 MHz and 10 MHz conductance curves which is reflected in an abrupt change of slope in the capacitance curves at about 1 V.

The sample prepared with low Ge content at 300°C (runs SG3 and SG4) exhibited essentially identical electrical behavior, indicating that the temperature at which the sample is loaded was not a significant factor at this stage of development of this process. The behavior of these samples is slightly superior to those of the 200°C from run SG1 (Figures 23(a) and 23(b)), as indicated by the fact that the low-frequency conductance peak of these samples, although slightly higher than in Figure 23(b), is substantially narrower (Figure 25(b)).

The sample prepared with higher Ge content (run SG2) exhibits much worse electrical properties than either the baseline Si_3N_4 film or silicon germanium nitride films with lower Ge content.

Thus our initial attempts to produce films of silicon germanium nitride did not result in improvements of the interfacial electrical properties over those obtained by the baseline PED silicon nitride process. The initial results appear to indicate that the interfacial properties degrade with increasing Ge content.

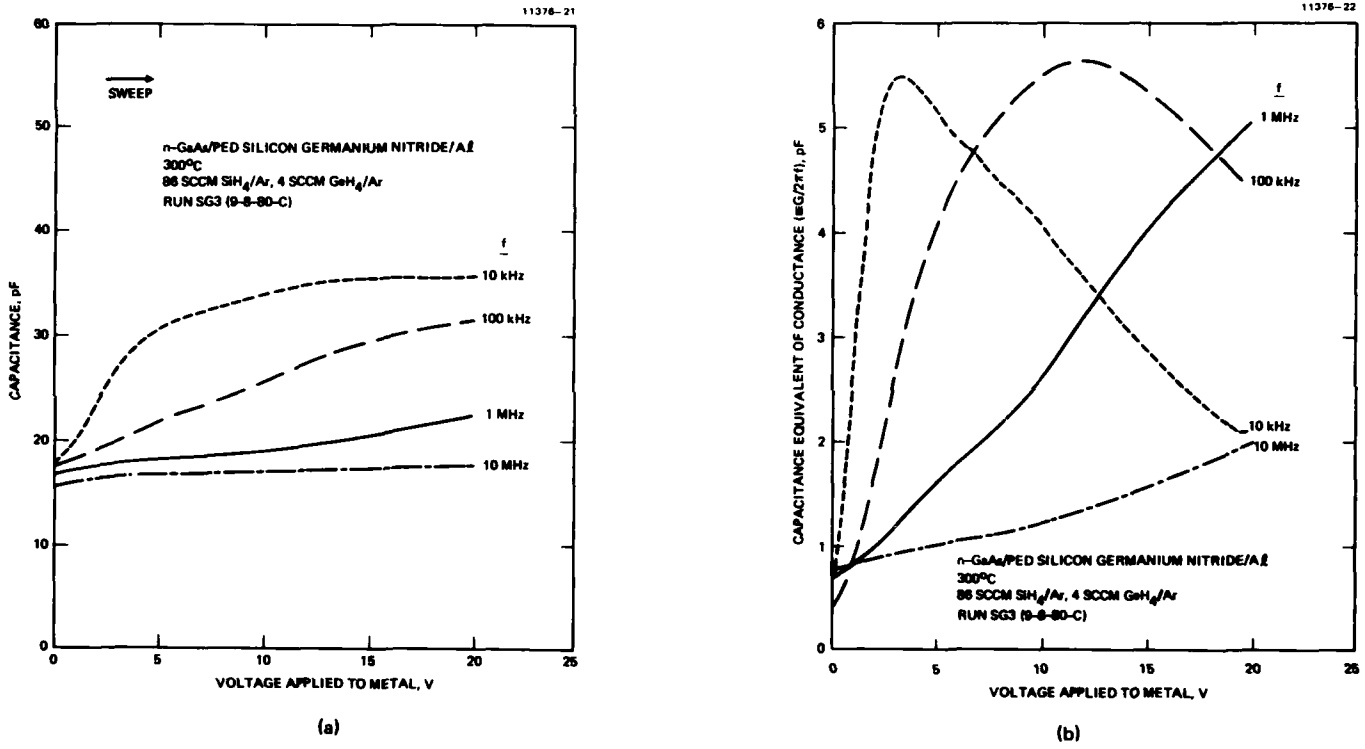


Figure 25. Electrical characteristics of an n-GaAs/PED silicon germanium nitride/Al capacitor employing a dielectric deposited at 300°C with gas flows of 16 sccm N_2, 86 sccm of 1.5% SiH_4 in Ar and 4 sccm of 1.5% GeH_4 in Ar, with no preburn. (a) Capacitance-voltage characteristics, (b) Conductance-voltage characteristics.

SECTION 7

PYROLYTIC CHEMICAL VAPOR DEPOSITION OF GERMANIUM NITRIDE

During the last six months of this program, 17 deposition runs were performed in an unsuccessful attempt to deposit Ge_3N_4 by pyrolytic reaction of germane with ammonia.

Feed gases for the CVD Ge_3N_4 runs were 1.5% GeH_4 in Ar, NH_3, and N_2 carrier gas. All depositions were done on Si substrates only in an attempt to determine satisfactory deposition parameters. Flow rates chosen as a starting point were those used for Si_3N_4, with the flow rate of 1.5% GeH_4 in Ar increased to compensate for the greater dilution compared to the 5% SiH_4 in N_2 used for Si_3N_4 deposition. The initial deposition temperature was 600°C. Films deposited under these conditions were of metallic appearance and were judged to be extremely Ge-rich. In the course of this investigation, the relative NH_3/GeH_4 ratio was increased by a factor of 65, the carrier gas flow was reduced by a factor of 2, and the temperature was varied over the range 400 to 600°C without successful deposition of Ge_3N_4. Based upon ellipsometric parameters and visual examination, the results were judged to vary from highly Ge-rich GeN_x to relative pure Ge. Hence we concluded that the reaction $GeH_4 + NH_3$ is unsuitable for deposition of Ge_3N_4 in our CVD reactor and we abandoned this approach.

SECTION 8

CONCLUSIONS

During the course of this program we explored a number of avenues toward the elusive goal of developing surface passivation techniques suitable for the development of a GaAs insulated gate device technology. Our early experiences with deposited oxides and with oxygen contaminated nitrides were consistent with the presently generally accepted hypothesis that the presence of substantial concentrations of oxygen at the GaAs/insulator interface leads to poor interface electrical properties.

The apparent incompatibility of oxygen with adequate GaAs surface passivation necessarily leads to the exploration of oxygen-free dielectrics. We believe that the nitride systems originally proposed for work on this program — silicon nitride, germanium nitride, and silicon germanium nitride — were very reasonable choices and warrant further investigation.

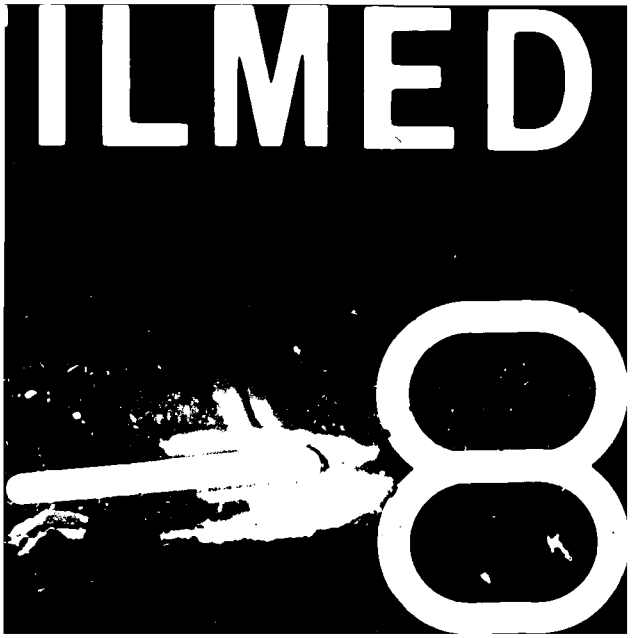
Of these three nitride systems, silicon nitride is by far the most tractable with which to work. Silicon is sufficiently highly reactive that it is relatively straightforward to prepare silicon nitride with approximately stoichiometric silicon-to-nitrogen ratios by pyrolysis or by low-temperature plasma-enhanced-deposition given adequate equipment. Using Hughes internal funds concurrently with this program we have demonstrated that it is possible to construct a plasma-enhanced deposition system that can prepare essentially oxygen-free silicon nitride films with thickness uniformity adequate for integrated circuit applications over large area substrates ($\pm 1.25\%$ over a 5 cm diameter wafer). Pyrolytic chemical vapor deposition of stoichiometric Si_3N_4 is possible at temperatures as low as 615°C given adequately leak-tight equipment.

Germanium nitride (and silicon germanium nitride) deposition on the other hand, is much more troublesome than silicon nitride deposition. We have found it essentially impossible, even with state-of-the-art equipment, to prepare oxygen-free, stoichiometric germanium nitride. Our films have generally exhibited substantial oxygen contamination and have generally been germanium-rich (and hence relatively conductive). Considering the oxygen content of our germanium nitride films, the quality of the interface electrical properties

our n-GaAs/PED germanium nitride/Al MIS capacitors is really quite remarkable. This fact alone is a strong impetus to seek superior techniques for preparation of germanium nitride films. Perhaps given a truly ultra-high vacuum compatible system plasma-enhanced deposition of oxygen-free germanium nitride films on GaAs surfaces could be achieved. Improved stoichiometry might be achieved by using more active reagents than ammonia (e.g., hydrazine).

Returning to the more tractable system, PED silicon nitride, our parametric study has clearly identified two areas in which further exploration would be most highly profitable: (1) treatment of the GaAs surface prior to deposition with reducing agents such as the hydrogenated species studied to date, and (2) post-deposition thermal annealing of GaAs/insulator samples. Our few preliminary annealing studies resulted in substantial improvements in interfacial electrical properties and showed clearly that the post-anneal electrical characteristics depend strongly on the pre-deposition surface treatment of the GaAs surface. Further exploration in these areas is clearly warranted.

*U.S.Government Printing Office: 1982 — 559-004/3032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